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RESEARCH ARTICLE

ADVANCED DIGITAL SIGNAL PROCESSING TECHNIQUE TO REDUCE SYSTEM COMPLEXITY USING DHT ALGORITHM

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Abstract—In this paper a new very large scale integration (VLSI) algorithm for a 2N-length discrete Hartley transform (DHT) that can be efficiently implemented on a highly modular and parallel VLSI architecture having a regular structure is presented. The DHT algorithm can be efficiently split on several parallel parts that can be executed concurrently. In this we present a new approach to design VLSI algorithms and VLSI architectures based on a synergistic treatment of the problems at algorithmic, architectural and implementation level. Moreover, the proposed algorithm is well suited for the sub expression sharing techniques that can be used to significantly reduce the hardware complexity of the highly parallel VLSI implementation and also it will increase the speed of the parallel multipliers. Using the advantages of the proposed algorithm and the fact that we can efficiently share the multipliers with the same constant, the number of the multipliers has been significantly reduced such that the number of multipliers is very small comparing with that of the existing algorithms. Thereby, the cost and power of the design can be reduced both in efficient implementation of transforms and reduction/removal of intermediate stages by employing different techniques. The performance overview of our proposal is that we will have efficiently replacing an faster adder and high speed multiplier in the existing algorithm of highly modular and parallel architecture, thereby resulting in significant reduction of overall power consumption, propagation delay, increases the speed and improves the overall hardware complexity of the system.

Index Terms—Discrete Hartley transform (DHT), DHT domain processing, Multiplier, fast algorithms

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