Available Online at www.ijcsmc.com

International Journal of Computer Science and Mobile Computing

A Monthly Journal of Computer Science and Information Technology

ISSN 2320–088X

IJCSMC, Vol. 3, Issue. 3, March 2014, pg.837 – 844

REVIEW ARTICLE

Review on Design and Implementation of DSSS-CDMA Transmitter using HDL with Raised Cosine Filter to Minimize ISI

Md. Sohrab Ansari[1], Mathew Oommen[2], Velmurugan.S[3]

[1]M.Tech. Scholar, Dept. of ECE, Hindustan University, Chennai, India
[2]M.Tech. Scholar, Dept. of ECE, Hindustan University, Chennai, India
[3]M.Tech. Scholar, Dept. of ECE, Hindustan University, Chennai, India

[1] sohrab.ete@gmail.com; [2] mathewoommen91@gmail.com; [3] velsrt@gmail.com

---

Abstract— Spread spectrum technology has blossomed from a military technology into one of the fundamental building blocks in current and next-generation wireless systems.* The *spread-spectrum technology provides antijam capabilities through a processing gain that results from using a wideband (large bandwidth) signal and it also provides capacity enhancement and robustness against noise. This paper presents the design and implementation of a direct sequence spread spectrum (DSSS-CDMA) system using HDL. The transmitter module mainly consist of symbol generator, PN sequence generator, spreader and BPSK modulator, IF carrier generator ,Root cosine filter(RCF) and DAC (Digital to Analog Convertor) blocks. The Xilinx Synthesis Technology (XST) of Xilinx ISE (Integrated Software Environment) 14.7 version tool will be used for synthesis of transmitter on FPGA(Field Programmable Gate Array) and also MATLAB(R2012b) software will be used for simulation purpose. To minimize the inter-symbol interference (ISI) at transmitter side the Raised cosine filtering will be performed.

Keywords— DSSS-CDMA, VHDL, BPSK, Spread Spectrum, ISI, FPGA, RCF, DAC

Full Text: http://www.ijcsmc.com/docs/papers/March2014/V3I3201499b28.pdf