Available Online at www.ijcsmc.com

International Journal of Computer Science and Mobile Computing

A Monthly Journal of Computer Science and Information Technology

ISSN 2320–088X

IJCSMC, Vol. 2, Issue. 5, May 2013, pg.33 – 40

RESEARCH ARTICLE

MULTIPLE FAULT DIAGNOSIS FOR HIGH SPEED HYBRID MEMORY ARCHITECTURE

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Abstract— This paper presents a built-in self-test (BIST)-based scheme for fault diagnosis that can be used to identify permanent failures and automatic correction in all memories & circuits. The proposed approach offers a simple test flow and does not require intensive interactions between a BIST controller and a tester. The scheme rests on partitioning of rows and columns of the memory array by employing low cost test logic. It is designed to meet requirements of at-speed test thus enabling detection of timing defects.

Key Terms: - Built-in self-test (BIST); deterministic partitioning; discrete logarithms; embedded read-only memory; fault diagnosis

Full Text: http://www.ijcsmc.com/docs/papers/May2013/V2I5201322.pdf