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RESEARCH ARTICLE

FPGA PROTOTYPING OF UNIVERSAL ASYNCHRONOUS RECEIVER TRANSMITTER (UART) WITH LOW POWER TPG BASED BIST ARCHITECTURE

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Abstract—A digital system is tested and diagnosed during its lifetime on numerous occasions. Test and diagnosis must be quick and have very high fault coverage. One way to ensure this is to specify test as one of the system functions, so it becomes self-test. With properly designed BIST, the cost of added test hardware will be more than balanced by the benefits in terms of reliability and reduced maintenance cost. This paper presents a low power test pattern generator for BIST without affecting the fault coverage. The proposed test pattern generator reduces the switching activity among the test patterns. This BIST scheme is evaluated with Universal Asynchronous Receiver and Transmitter (UART) as Circuit under Test. The 8-bit UART with status register and low power TPG based BIST module is coded in Verilog HDL and synthesized and simulated using Xilinx XST and ISim version 14.6 and realized on Spartan 3E FPGA.

Index Terms—Built-In-Self-Test (BIST), LP-LFSR, UART, FPGA

I. INTRODUCTION

In VLSI circuits, built in self-test (BIST) are used for testing. The objective of the BIST is to reduce power dissipation without affecting the fault coverage. The main challenging areas in VLSI circuits are cost, performance, reliability, power, testing and area. The demand for portable computing devices and communication system are rapidly increasing. These applications require low power dissipation for VLSI circuits [1]. The ability to design, fabricate and test Application Specific Integrated Circuits (ASICs) as well as FPGAs with gate count of the order of a few tens of millions has led to the development of complex embedded SOC. Hardware components in a SOC may include one or more processors, memories and dedicated components for accelerating critical tasks and interfaces to various peripherals. One of the approaches for SOC design is the platform based approach. The platform FPGA includes custom designed fixed programmable processor cores together with millions of gates of reconfigurable logic devices.

In addition to this, the development of Intellectual Property (IP) cores for the FPGA's for a variety of standard functions including processor's, enables a multimillion gate FPGA to be configured to contain all the hard-core processors and they can be enhanced with custom hardware to optimize them for specific application. Power dissipation is a challenging problem for today's System-on- Chips (SOCs) design and test.

The power dissipation in CMOS technology is either static or dynamic. Static power dissipation is primarily due to the leakage currents and contribution to the total power dissipation is very small. The dominant factor in the power dissipation is the dynamic power which is consumed when the circuit nodes switch from 0 to1. During switching, the power is consumed due to the short circuit current flow. Four reasons are blamed for power increase during test: (1) High-switching activity due to nature of test patterns, (2) Parallel activation of internal cores during test, (3) Power consumed by extra design-for-test (DFT) circuitry, (4) Low correlation among test vectors.

The power dissipation of a system in test mode is more than in normal mode. Low correlation between consecutive tests happens when applying low correlated patterns to scan chains. Increase in switching activity in scan chain results in increased power consumption in scan chain and combinational block. This extra power consumption (average or peak) can create problems such as instantaneous power surge that cause circuit damage, formation of hot spots, difficulty in performance verification, and reduction of the product yield and lifetime. Different types of techniques are presented in the literature to control the power consumption. These mainly includes algorithms for test scheduling with minimum power, techniques to reduce average and peak power, techniques for reducing power during scan testing and BIST(built-in-self- test) technique. Since off-chip communication between the FPGA and a processor is bound to be slower than on- chip communication, in order to minimize the time required for adjustment of the parameters, the built in self- test approach using design for testability technique is proposed for this case.

As ICs grow in gate counts, it is no longer true that most gate nodes are directly accessible by one of the pins on the package. This makes testing of internal nodes more difficult as they could neither no longer be easily controlled by signal from an input pin (controllability) nor easily observed at an output pin (observe ability). Hence Internal Diagnostic Capabilities are to be introduced to test the embedded cores.
In this paper, internal diagnostic capabilities are built into UART by the introduction of Built-In-Self-Test (BIST) [2] and error simulation of data at receiver for any data corruption and thereby setting status flags [3]. The UART with status register and BIST module is coded in Verilog HDL and simulated using Xilinx tool ISim. The complete implementation and validation is done on Spartan 3E FPGA.

The rest of the paper is organized into 6 sections. Section II literature survey relevant to power reduction are explained, mainly concentrated to reduce the average and peak power. In section III the proposed technique in the test pattern generator is described. Section IV explains the architecture of UART with introduction of BIST technique. Simulations results of each module using Xilinx ISim Simulator are illustrated in Section V and section VI provides the conclusion of work.

II. LITERATURE SURVEY

Different techniques are available to reduce the switching activities of test pattern, which reduce the power in test mode. Y.Zorian [4] presented that the power dissipation of a system in test mode is more than in normal mode. Mechrdad Nourani [5] explained that this extra average power consumption and peak power consumption can create problems such as instantaneous power surge that cause formation of hot spots, circuit damage, difficulty in performance verification and reduction of the product field and life time. Thus, special care must be taken to ensure that the power rating of circuits is not exceeded during test application. Different types of methods are stated to control the power consumption. These methods mainly includes algorithms for test scheduling with minimum power, techniques to reduce peak power and average power, techniques for reducing power during scan testing and BIST(built-in-self-test) technique. In order to minimize the time required for adjustment of the parameters, off-chip communication between a processor and the FPGA is bound to be slower than on-chip communication. The BIST (built-in-self-test) approach using design for testability technique is presented for this case.

Different techniques are available to reduce the switching activities of test pattern, which reduces the power in test mode. P. Giard [6] proposed a modified clock scheme for linear feedback shift register (LFSR), in which only half of the D flip-flops works. Thus, only half of the test pattern can be switched. S.K.Guptha [7] determined a BIST TPG for low switching activity in which there is d-times clock frequency between slow LFSR and normal LFSR and thus, the test pattern generated by original LFSR is re-arranged to reduce the switch frequency. Mechrdad Nourani [5] presented low transition test pattern generator (LT-TPG) which reduces the average and peak power of a circuit during test. The above said techniques can reduce the average power compared to traditional linear feedback shift register (LFSR).

A better low power can be achieved by using single input change pattern generators. I.Voyiatzis et al., [8] and S.C.Lei et al.,[9] demonstrated that the combination of scan shift register and LFSR are used to generate random single input change sequences. S.C.Lei et al., [9] and R.H. He et al., [10] proposed that (2m-1) single input change test vectors can be inserted between two adjustment vectors generated by LFSR where m is length of LFSR. Bo Ye and Tian-Wang Li [11] proposed that 2m single input changing data is inserted between two neighboring seeds. The average and peak power are reduced by using the above techniques. Still, the switching activities will be large when clock frequency is high.

III. PROPOSED LOW-POWER TEST PATTERN GENERATOR

Linear feedback shift register [LFSR] is used due to the simplicity of the circuit and less area occupation, for generating test patterns. In this paper, we determined a novel architecture which generates the test patterns with reduced switching activities. Figure 1 shows the Low power test pattern generator (LP-TPG) structure consists of modified low power linear feedback shift register (LP-LFSR), m-bit counter, gray code generator, NOR-gate structure and XOR array.

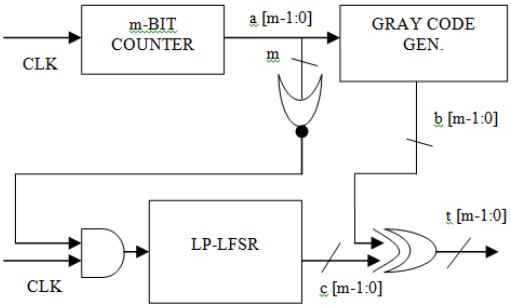

Fig.1 Low power test pattern generator

The m-bit counter is initialized with Zeros and which generates 2m test patterns in sequence. A gray code generator and m-bit counter are controlled by common clock signal [CLK]. The output of m-bit counter is applied as input to a NOR-gate structure and a gray code generator. When all the bits of counter output are Zero, the NOR-gate output is one. Only when the NOR-gate output is one, the clock signal is applied to activate the LP-LFSR which generates the next sequence. The sequence generated from LP-LFSR is Exclusive–ORed with the sequence generated from gray code generator. The patterns generated from the Exclusive–OR array are the final output patterns.

IV. UART ARCHITECTURE WITH BIST

A properly designed BIST is able to offset the cost of added test hardware while at the same time ensuring the reliability, testability and reduces maintenance cost. BIST solution consists of a Test

Pattern Generator (TPG), the circuit to be tested, a way to analyze the results, and a way to compress those results for simplicity and handling. Fig. 2 shows a BIST module composition. Generic BIST architecture components [7] are;

Circuit under Test (CUT): This is the portion of the circuit tested in BIST mode. It can be sequential, combinational or a memory. It is delimited by their Primary Input (PI) and Primary Output (PO).

Test Pattern Generator (TPG): It generates the test patterns for the CUT. It is a dedicated circuit or a microprocessor.

The patterns may be generated in pseudorandom or deterministically. Normally, the pattern generator generates exhaustive input test patterns to the CUT to ensure the high fault coverage. For example, a CUT with 10 inputs will require 1024 test patterns.

Test Response Analysis (TRA): It analyses the value sequence on PO and compares it with the expected output.

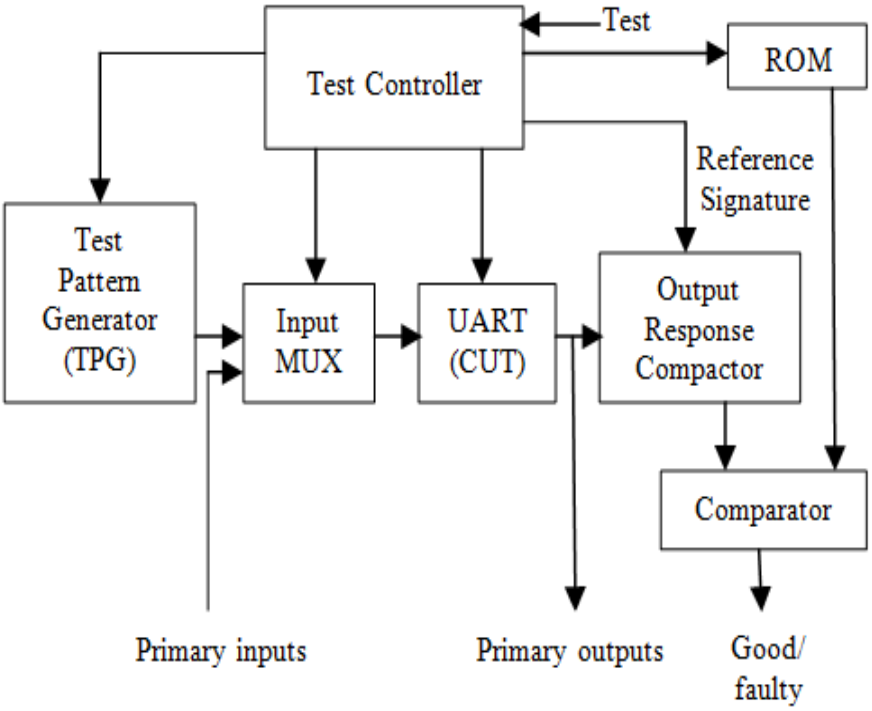

Fig.2 BIST architecture block diagram

The architecture proposes an 8-bit UART which operates at a baud rate of 9600 bps with a status register to monitor the correctness of every received data byte and enhance the testability of circuit by the introduction of BIST module. The hardware architecture of the 8-bit UART with Status register, incorporated with BIST module is explained in the following sections.

The proposed model has two major modules viz. UART and BIST. Further in the UART, we have transmitter, receiver, and baud rate generator. Baud rate generator works at 50 MHz and further reduced as required for the operations in transmitter and receiver to achieve baud rate of 9600 bps.

A. UART Transmitter

The transmitter accepts parallel data from peripheral/processor, makes the frame of the data and transmits the data in serial form on the Transmitter Output (TXOUT) terminal (fig. 3). The baud rate generator output will be the clock for UART transmitter.

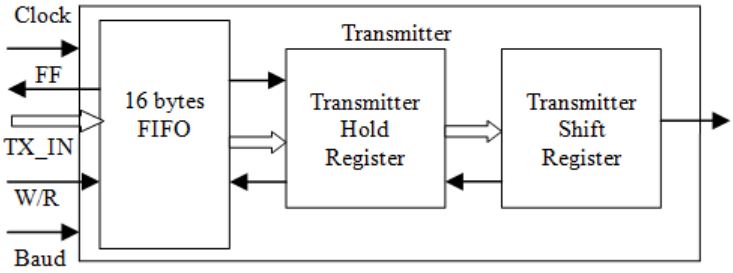

Fig.3 UART Transmitter

Data is loaded from the parallel inputs TXIN0-TXIN7 into the Transmitter FIFO by applying logic high on the W/R (Write) input. FIFO is 16-byte register. If FIFO is full, it sends FIFO Full (FF) signal to peripheral.

When FIFO contains some data, it will send the signal to Transmitter Hold Register (THR), which is an 8-bit register. At the same time, if THR is empty it will send the signal to FIFO, which indicates that THR is ready to receive data from FIFO. If Transmitter Shift Register (TSR) is empty, it will send the signal to THR and it indicates that TSR is ready to receive data from THR. TSR is an 11-bit register in which framing process occurs. In frame, start bit, parity bit and one stop bit will be added. Now data is transmitted from TSR to TXOUT serially.

B. UART Receiver

The received serial data is available on the RXIN pin. The received data is applied to the sampling logic block. The receiver timing and control is used for synchronization of clock signal between transmitter and receiver. The receiver sampling is 8 times to that of the transmitter baud rate. In the architecture of UART receiver as shown in fig 4, initially the logic line (RxIn) is high.

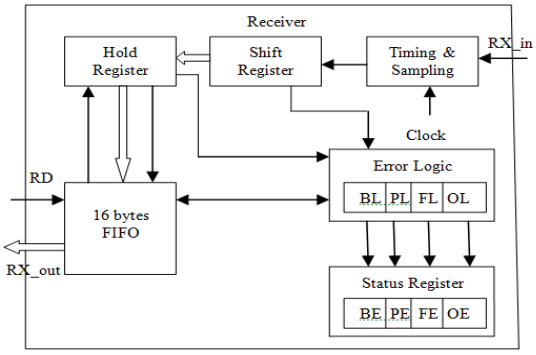

Fig. 4 UART Receiver

Whenever it goes low sampling and logic block will take 4 samples of that bit and if all four are same it indicates the start of a frame. After that remaining bits are sampled in the same way and all the bits are send to Receiver Shift Register (RSR) one by one where the entire frame is stored. RSR is a 11 bit shift register.

Now if the Receiver Hold Register (RHR) is empty it sends signal to RSR so that only the data bits from RSR goes to RHR which is an 8 bit register. The remaining bits in the RSR are used by the error logic block. Then, if receiver FIFO is empty it send the signal to RHR so that the data bits goes to FIFO. When RD signal is asserted the data is available in parallel form on the RXOUT0-RXOUT7 pins.

The status register is implemented with flags for error logic operations performed on the received data. The error logic block handles 4 types of errors: Parity error (PE), Frame error (FE), Overrun error (OE), Break error (BE). If the received parity does not match with the parity generated from data bits, PE bit will be set which indicates that parity error occurred. If receiver fails to detect correct stop bit or when 4 samples do not match frame error occurs and FE bit is set. If the receiver FIFO is full and other data arrives at, RHR overrun error occurs and OE bit is set. If the RXIN pin is held low for long time than the frame time then there is a break in received data and break error occurs and BE bit is set.

V. SIMULATION RESULTS

The 8-bit UART with status register and low power TPG based BIST module is coded in Verilog HDL and synthesized and simulated using Xilinx XST and ISim version 14.6 and realized on Spartan 3E FPGA.

A. Simulation results of Conventional LFSR

The fig 5 shows the simulation results of conventional LFSR in which the LFSR is loaded with initial value 10010001 during reset. Random test patterns are generated when reset is low.

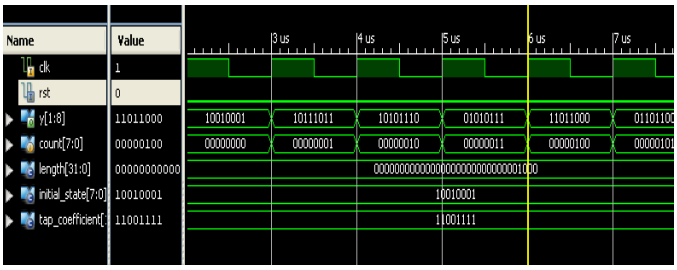

Fig.5 Simulation results of Conventional LFSR

B. Simulation results of LP-LSFR

The fig 6 shows the simulation results of LP-LFSR. The random patterns generated from this LSFR have less switching activity compared to conventional LFSR.

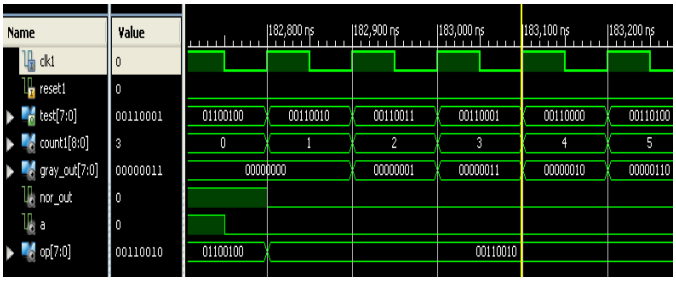

Fig.6 Simulation results of LP-LSFR

C. Simulation results of UART Transmitter

The fig.7 shows the serial transmission of data. First data being transmitted is "11001110". This 8-bit data is loaded to transmit shift register and start, stop & parity bits are added to form the frame inside TSR and sent to TXD.

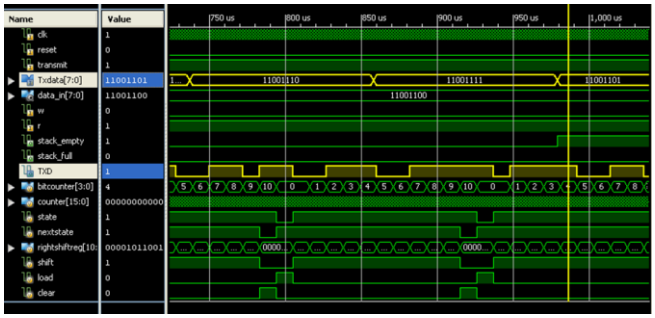

Fig.7 Simulation results of UART Transmitter

When the reset is 0 and transmit is 1, the transmitter starts transmitting the data, i.e. the data starts shifting out from the transmitter shift register. Since the desired baud rate is 9600bps, the bits are shifted out on TxD line at the interval of 50MHz/9600=5208 clock cycles. Similarly all the bits are sent. The serial transmission is observed at TXD pin along with frame format (1 logical low start bit, 8-bit data (LSB to MSB), parity bit and finally logical high stop bit).

D. Simulation results of UART Receiver

The UART receiver converts the serial data into parallel form and makes it available at RxData [7:0]. The Serial data is received at RXD pin. Each bit is sampled and the sampled bit is saved into receive shift register. From this, the frame bits viz. start, parity and stop bits are discarded in RSR and written to receive FIFO, RxData. The 8-bit data simulated is "11001110". Further received data will be stored in the remaining FIFO locations. Fig. 8 shows the reception of serial data. We can also observe from the fig.8 the parity error, break error and stop-bit error are set to logic low confirming no error in the received data.

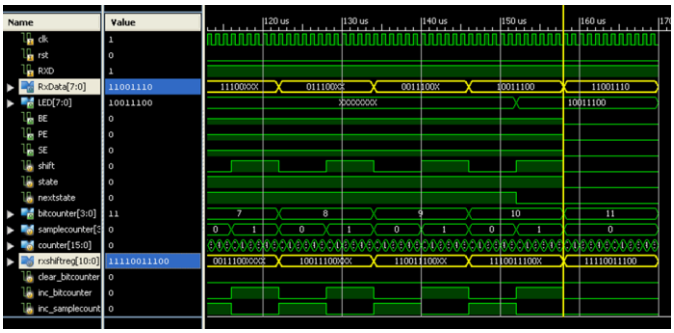

Fig.8 Simulation results of Receiver

E. Simulation results of UART with BIST Architecture

The fig.9 shows the simulation results of UART implementation with low-power BIST architecture. Low power test patters are transmitted from the transmitter to receiver. These test patterns are received at the receiver side and they are compared with the expected test pattern values.

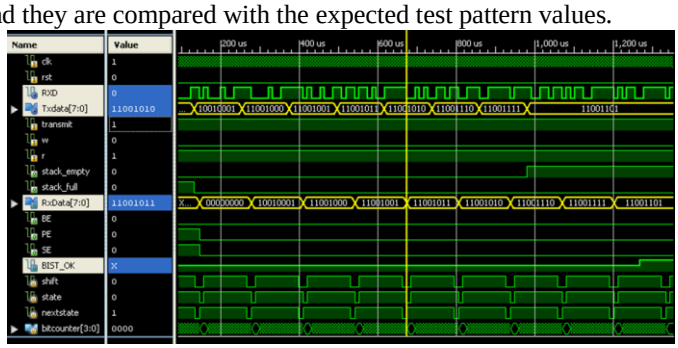

Fig.9 Simulation results of UART with BIST architecture

If they match the BIST operation is complete and the circuit under test which is the UART is tested ok. From the fig.9 we can see the BEST_OK is set high indicating successful operation of BIST for UART.

F. FPGA Implementation results of UART with BIST Architecture

The UART is implemented on Spartan 3E XC3S500E FPGA running at 50 MHz clock along with the implementation of FIFO and BIST architecture. The test patterns are generated, transmitted and compared to verify the proper operation of UART. In fig.10 the right most LED is set high indicating the UART is tested and circuit under test is working well.

Fig.10 FPGA Implementation results of UART with BIST Architecture

VI. CONCLUSION

The architecture of UART that support 8-bit data word length at 9600 bps baud rate for serial transmission of data with the addition of status register for detecting errors in data transfer and BIST which allows to test the circuit itself, is introduced. Working of UART has been tested using Xilinx ISim 14.6, which is implemented on FPGA. With error checking status register, we can detect the different types of errors occurred during communication and hence correct them.

An efficient low power test pattern generator (LP-TPG) method had been proposed to reduce the test power and uses a modified pseudo-random pattern generator to produce seeds and then operates with the single input changing generator and an exclusive-OR array, thus pseudo-random signal input changing sequences are generated, which effectively reduces the switching activities between the test patterns. Thus, the proposed method reduces the power consumption during testing mode with minimum number of switching activities using LP-LFSR instead of conventional LFSR.

REFERENCES

[1] BalwinderSingh, Arun khosla and Sukhleen Bindra "Power Optimization of linear feedback shift register(LFSR) for low power BIST", 2009 IEEE international Advance computing conference(IACC 2009) Patiala,India 6-7 March 2009.

[2] Fang Yi-yuan and Chen Xue-jun, "Design and Simulation of UART Serial Communication Module Based on VHDL", in the proceedings of 3rd International Workshop on Intelligent Systems and Applications (ISA), IEEE, May 2011, DOI: 10.1109/ISA.2011.5873448, pp.1-4.

[3] Naresh, Vatsalkumar and Vikaskumar Patel, "VHDL Implementation of UART with Status Register", in the proceedings of International Conference on Communication Systems and Network Technologies, IEEE Computer Society, 11-13th May 2012, DOI: 10.1109/CSNT.2012.164, pp.750-754.

[4] Y.Zorian, "A Distributed BIST control scheme for complex VLSI devices," Proc. VLSI Test Symp., P.4-9,1993.

[5] P. Mechrdad Nourani, "Low-transition test pattern generation for BIST Based Applications", IEEE TRANSACTIONS ON COMPUTERS, Vol 57,No.3 ,March 2008.

[6] P.Girard, L.Guiller, C.Landrault, S.Pravossoudovitch,and H.J.Wunderlich," A modified clock scheme for a low power BIST test pattern generator," 19th IEEE proc. VLSI test Symp.,CA,pp-306-311,Apr-May 2001.

[7] Y. S.Wang and S.K.Gupta,"DS-LFSR: a BIST TPG for low switching activity," IEEE Trans.computer-aided design of Integrated circuits and systems, Vol. 21,No.7,pp.842-851,July 2002.

[8] I.Voyiatzis,A.paschalis,D.Nikolos and C.Halatsis, "An efficient built-in self-test method for robust path delay fault testing," Journal of electronic testing: Theory and applications Vol.8,No.2,pp-219-222,Apr- 1996.

[9] S.C.Lei, J.Guo, L.Cao, Z.Ye.Liu, and X.M.Wang,"SACSR: A low power BIST method for sequential circuits", Academic Journal of XI'AN jiaotong university (English Edition),Vol.20,no.3,pp.155- 159,2008.

[10] R.H.He,X.W.Li and Y.Z.Gong, " A scheme for low power BIST test pattern generator", micro-electronics & computer,no.2,pp.36-39 Feb.2003.

[11] Bo Ye and Tian-Wang Li,"A novel BIST scheme for low power testing", 3rd IEEE international conference, Vol.1,pp-134-137, July 2010 .

