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RESEARCH ARTICLE

REDUCING DYNAMIC POWER BY PULSED LATCH AND MULTIPLE PULSE GENERATOR IN CLOCKTREE

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Abstract: ***Nowadays power consumption is an important issue in high-performance digital circuits. Reducing Nowadays power consumption is an important issue in high-performance digital circuits. Reducing the size of a clock tree is an effective approach to reduce dynamic power dissipation in digital circuit designs. Existing methods are based on reduction of the flip-flop power alone, which gives limited amount of power savings. To achieve the considerable power saving, this project gives an analysis of the pulsed- latch utilization in a clock tree. A novel approach is proposed to efficiently construct a clock tree with both pulsed-latches and flip-flop. To avoid maximum power consumption in clock tree multiple pulse generators has been proposed. An algorithm has been developed for clock tree partition based on Voronoi diagram to avoid clustering. The method is based on minimum-cost, maximum-flow formulation to globally determine the tree topology, which maintains load balance and considers the wire length between pulse generators and pulsed latches. Experimental results indicate that the proposed novel approach can reduce the power consumption by a certain extent. It is an average compared with the most recent paper on the industrial circuits and ISCAS-2012 benchmarks respectively. This method simulated in Xilinx and Modelsim software.***
Keywords: ***clock tree size reduction, dynamic power reduction, pulse generator, pulsed latch***

Introduction

Power consumption has become a crucial issue in high-performance digital circuits. Several techniques are proposed to reduce total power of a chip, such as multiple supply voltages [1], clock gating [2]–[4] , and clock-tree minimization. Because of heavy pipeline designs and high-frequency signal switching, a clock tree is known to be a major contributor to power dissipation. The clock tree accounts for a significant portion of total power consumption and consumes 20%–40% of total power in synchronous circuits. Therefore, the chip power can be greatly reduced by decreasing the clock-tree power. The power dissipation of a clock tree can be reduced by decreasing total (clock) wire capacitance. However, existing methods of clock-tree minimization are primarily based on flip-flops and focus on wire length minimization alone, which may limit achievable power savings.

To avoid this problem, flip-flops are replaced with pulsed latch and latches are superior to flip-flops in terms of area, transition time, and power dissipation. The pulsed-latch designs have both advantages of latches and flip-flops:

- Timing verification is easy.
- Less power consumption

If all the flip-flops in the circuit are replaced by pulsed latch then the cost and physical complexity will increase. To avoid this drawback the proposed method replaces a few flip flops with pulsed latch in the clock

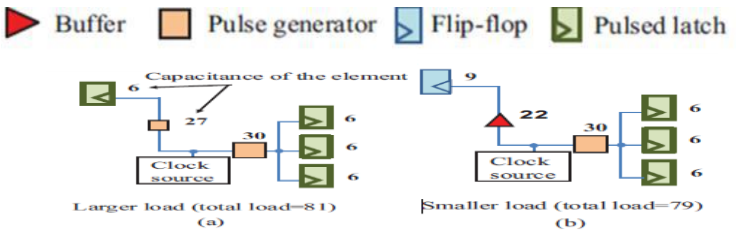
tree design. So the proposed clock tree method contain both flip flop and pulsed latch to reduce the considerable power saving.

I. Pulsed Latch Concept

In current circuit designs, the most common storage element is a D-type flip-flop that consists of two latches (master and slave) triggered by a clock signal. As transistor counts of a flip-flop are two times than that of a single latch, latches are superior to flip-flops in terms of area, transition time, and power dissipation. A pulsed-latch-based design style was adopted for dynamic power reduction. However, this modification obtain excessive costs and causes high complexity in physical-synthesis stages. Therefore, in this paper, we present an efficient pulsed-latch approach in physical design to minimize the cost of utilizing pulsed latches under the current design flow. The proposed method allows pulsed latches and flip-flops to design the clock tree.

Therefore, the clock tree with mixture of sinks is constructed to further reduce power dissipation, which consumes less power than that of the clock tree shown in Figure 1(a). As Figure 1(b) shows, one sink is not replaced by the pulsed latch, and the clock tree has a mixture of sinks (flip-flops and pulsed latches) for further power reduction.

Figure 1. Clock tree with different types of sinks and drivers

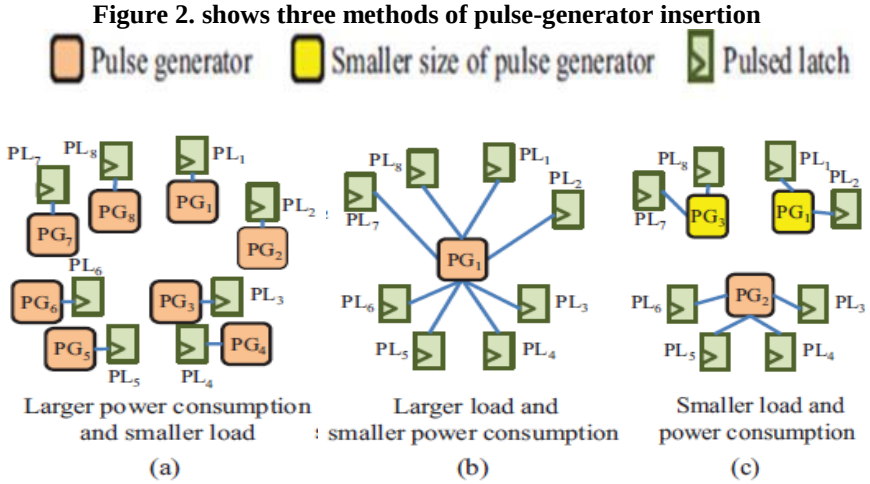


II. Pulsed Latch Replacement And Pulse Generator Insertion

Since the pulse generator should be inserted in the clock network which considering the trade-off of power consumption between pulse generators and pulsed latch, the methodology employs one objective function in clock tree synthesis (CTS) methodology to pick up a clock-tree structure with the most efficient power reduction through pulsed latch replacement. Pulsed latches can then be used to substitute existing flip-flops where ever such substitution is possible. Thus, there is a tradeoff between the pulse-generator insertion and pulsed-latch substitution. As the clock pulse is sensitive to output load, it is essential to control the load of a pulse generator for potential pulse degradation. Therefore, two major factors must be considered to control the output load:

1) The pulse-generator driving load cannot exceed the maximum tolerable load defined in the library and
2) The number of pulsed latches driven by a pulse generator should be smaller than the maximum fan out number.

Figure 2. shows three methods of pulse-generator insertion



To prevent the distortion of a clock signal, a pulse generator connects a single pulsed latch in [Figure 2(a)], but the power consumption may be significantly high, because of the many inserted pulse generators. On the other hand, if we use a single pulse generator to drive all pulsed latches [Figure 2(b)], the clock pulse waveform may be degraded because of a heavy output load or maximum fan out constraint.

Considering the tolerable load of a pulse generator, the result with the best trade off in this example is to use three pulse generators to trigger pulsed latches [Figure 2(c)]. The two upper pulse generators *PG*1 and *PG*3 in

Figure 2(c) can be replaced by a smaller-size one (yellow) because it only drives two pulsed latches, further reducing power consumption.

IV. Design Flow

Figure 3. Comparisons of pulsed-latch design flows. (a) Design flow with pulsed latch alone (b) Proposed design flow with mixed structure

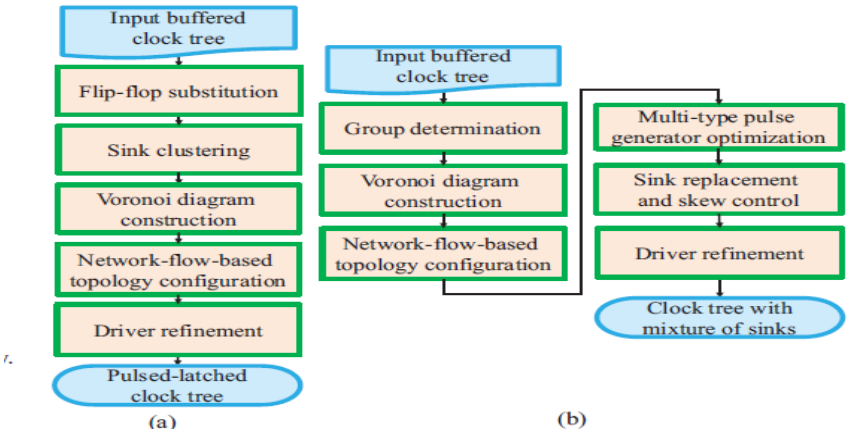


Figure 3 shows a comparison between previous existing design and the proposed design. As Figure 3(a) shows, presented a pulsed-latch with a single-type pulse generator. However, this proposed method should contain a mixed structure of pulse latches and flip-flops. Moreover, the driven load of pulse generators may be different, and replacing generators with smaller generators will further reduce power consumption. To achieve these goals, this paper presents a new clock tree with a mixed structure of pulse latches and flip-flops that is capable of multi type pulse-generator insertion [Figure 3(b)].

V. Voroni Diagram Construction

As pulsed-latch-aware clustering always merge the closest sinks, the results could exclude some better solutions. To overcome this deficiency, In a Voronoi diagram, for each pulsed latch within a convex polygon, the distance between the pulsed latch and its original pulse generator may be farther than the distance between pulse generators located in other polygons and itself.

Therefore, a pulsed latch located at neighboring polygons may connect to the corresponding nearest pulse generator, such that pulsed latches can be collectively considered when determining the topology.

Figure 4. Example of connecting pulsed latches to nearest inserted pulse generators.

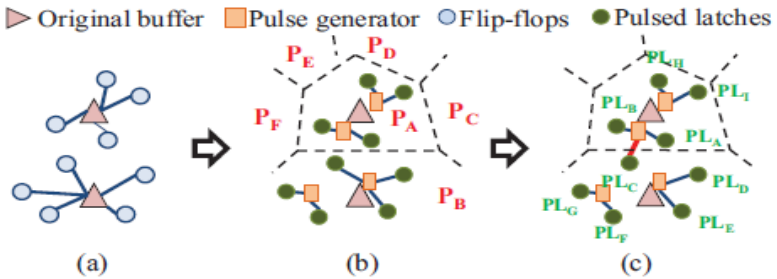


Figure 4 shows an example of pulsed latches connected to the nearest inserted pulse generator. Initially, two lowest-level buffers connect to a set of flip-flops [Figure 4(a)]. Then, use the original buffers to construct a Voronoi diagram and replace the flip-flops with pulsed latches clustered by pulsed-latch-aware clustering [Figure 4 (b)]. Dotted lines indicate the Voronoi diagram, and there are six polygons (*PA* to *PF)*. Next, to group the nearest pulsed latches located at different polygons, we examine the distance between the pulsed latches in neighboring polygons and pulse generators.

When the polygon *PA* is selected to process, we will examine the pulsed latches at neighboring polygons and calculate the distance between the pulsed latches and the pulse generators in *PA*. The topology of pulsed latches and pulse generators changes if the wire length can be reduced without violating constraints. Figure 4(c) shows an example that *PLC* is at the boundary of polygon P_B, and PL_C is farther than the original pulse generator. This method groups the nearest pulse latches during topology determination.

VI. Major Goals of This Paper

1) Unlike most related papers, which are based on Flip-flops, the proposed method adopts pulsed-latch Utilization for power savings. This type of clock-tree Migration efficiently converts a flip-flop-based clock tree to a pulsed-latch-based clock tree.
2) Considering the additional power consumed by inserted Pulse generators, the proposed approach can efficiently construct a clock tree with both pulsed-latches and flip-flops.
3) To reduce runtime, the proposed approach uses a Voronoi diagram to divide the design into several Polygons for providing locality information among pulsed latches. We solve the problem with a minimum-cost maximum-flow method to globally determine the clock-tree topology, which maintains the appropriate load balance while considering the Wire length between pulse generators and pulsed latches.
4) Experimental results indicate that the proposed clock tree can reduce power consumption by 25% to 30% an average compared with the most recent paper on the industrial Circuits and ISCAS-2012 benchmarks, respectively.

VII. Power Analysis

We conducted experiments on ISCAS-2012 benchmarks, and compares the proposed clock tree with the Flip-flop-based and pulsed-latch-based trees. The comparison of power consumption and timing information are shown in table (1).These tables show the proposed approach can reduce the power consumption by25% to30%on average compared with flip-flop-based circuits and pulsed-latch-based circuits, respectively.

Table (1): power summary

BENCHMARK CIRCUIT	POWER COSUMPTION OF CIRCUITS USING FLIPFLOP	POWER COSUMPTION OF CIRCUITS USING PULSED LATCH
ISCAS 27	34mW	34mw
ISCAS208	119mw	79mw
ISCAS298	139mw	109mw

Figure 5. Power comparison chart

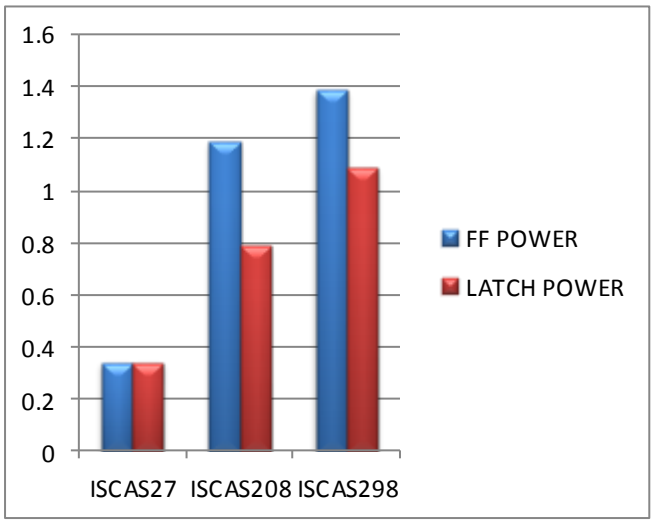
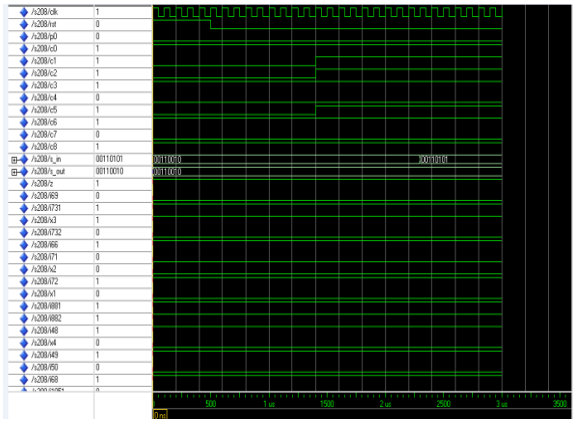


Figure 5 shows the power consumption of ISCAS-2012 Benchmark circuits. Proposed approach can reduce the power consumption by25% to30% on average compared with flip-flop-based circuits and pulsed-latch-based circuit.

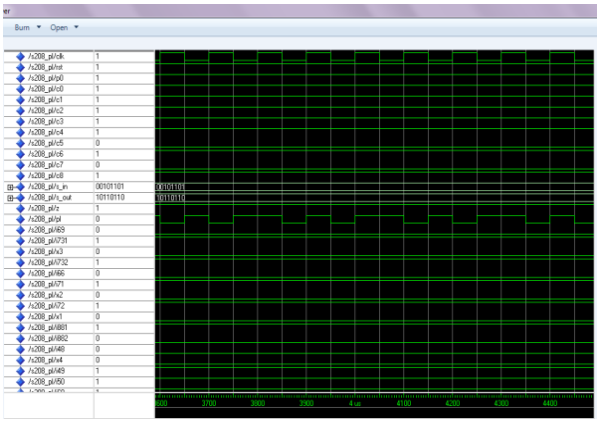
VIII. Simulation Result

The simulation result of ISCAS 2012 (ISCAS 208) benchmark circuit shown below:

Simulation result for ISCAS208 Circuit using Flipflop



Simulation result for ISCAS208 Circuit using Pulsed Latch

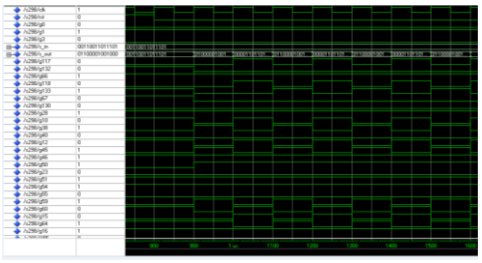


IX. Proposed Multiple Pulse Generator Method Insertion

To minimize clock power in digital circuits some of the flip flop in the circuit replaced with pulsed latch. The proposed clock approach based on both flip-flop and pulsed latch. In pulsed-latch designs, a pulse generator is indispensable to generate a clock pulse, but consumes more power than a pulsed latch and a buffer. As pulse generators consume large amounts of power in pulsed-latch circuits, it is critical to reduce the pulse-generator power. The proposed multi type pulse generator insertion reduces the unnecessary power dissipation. So the above benchmark circuits are implemented with multiple pulse generator instead of single pulse generator. These proposed methods again reduce the power consumption by 2% to 5% on average compared with single pulse generator.

The simulation result of ISCAS 2012 (ISCAS 344) benchmark circuit shown below:

Simulation result for ISCAS208 cCircuit using single pulse generator



Simulation result for ISCAS208 Circuit using multiple pulse generator

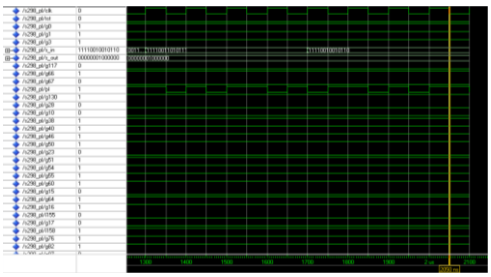


Figure 6. Power Comparison Graph

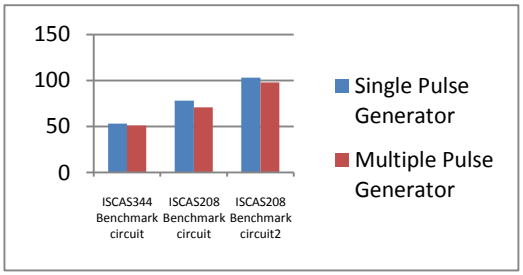


Figure 6 shows the power consumption of ISCAS-2012 Benchmark circuits. The migration approach can reduce the power consumption by25% to30%on average compared with flip-flop-based circuits and pulsed-

latch-based circuit. After these circuits are implemented with Multiple Generator .This proposed methods again reduce 2% to 5% power consumption.

X. Conclusion

In this paper, proposed an efficient clock-tree approach that replaces a flip-flop-based clock tree into a pulsed-latch-based one for dynamic power reduction. To further reduce the power dissipation of pulse generators, enabled multi type pulse generators and identified the pulse generators with suitable size to drive pulsed latches. Experimental results indicated that the proposed approach can improve both power consumption compared with the most recent research on the industrial circuits and ISCAS-2012 benchmarks, respectively.

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