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RESEARCH ARTICLE

LOW POWER REDUCED ROUTER NOC ARCHITECTURE DESIGN WITH CLASSICAL BUS BASED SYSTEM

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Abstract: Network-on-Chip (NoC) architectures represent a promising design paradigm to cope with increasing communication requirements in digital systems. Network-on-chip (NoC) has emerged as a vital factor that determines the performance and power consumption of many-core systems. A novel switching mechanism, called virtual circuit switching, is implemented with circuit switching and packet switching. A path allocation algorithm is used to determine VCS connections and circuit-switched connections on a mesh-connected NoC, such that both communication latency and power are optimized. The experimental results show that the hybrid scheme can efficiently reduce the communication latency and power. VCS connections and CS connections can be limited to the class of communications that need guaranteed latency, and packet switching can be used to serve the best effort traffic. To overcome this classical bus based system for NOC is proposed to reduce the number of switches and network interfaces to yield better latency and power consumption.

Key Words-Network-on-chip (NOC), Virtual circuit-switched (VCS) Connections, Classical bus based system.

I. INTRODUCTION

The increasing complexity of modern digital devices demands for ever increasing communication requirements, and for an ever increasing heterogeneity of the target applications. Specifically, different communication domains may be implemented using the same chip area, for instance to allow multiple parallel applications to be loaded onto the device.

Network-on-Chip (NoC) architectures represent a promising design paradigm to cope with increasing communi-cation requirements in heterogeneous digital systems. Classical design approaches, such as bus-based systems or point-to-point connections, are no longer suitable for highly integrated systems since they lack of flexibility and scalability with the increasing number of modules attached to the system. Nevertheless, NoC-based interconnects require additional design efforts and, in general, major resource requirements as compared to classical bus-based systems. Such an issue can be solved by directly optimizing over the different design factors. it achieved is low-resource usage communication architecture, meanwhile maintaining the desired performances.

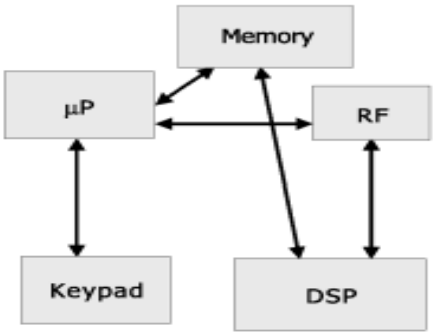
II. RELATED WORKS

A. Basics of network on chip architecture

The NoC architecture provides the communication infrastructure for the resources. It has two main objectives. Firstly, it is possible to develop the hardware of resources independently as stand-alone blocks and create the NoC by connecting the blocks as elements in the network. Secondly, the scalable and configurable network is a flexible platform that can be adapted to the needs of different workloads, while maintaining the generality of application development methods and practices.

B. Point-to-point interconnect

Simplicity is the major advantage of point–to-point interconnect the most significant drawback is that, the number of wire required grows rapidly as the number of channels increases by which the routing complexity is increased, moreover a point-to-point scheme also suffers from low wire utilization for low band width channels and a high hardware over head as dedicated interface for each channels are required .Here the memory is directly connected to DSP.



Fig(1).Point to point interconnect architecture.

C. Interconnect bus architectures

Bus architecture significantly reduces the total length of wires required and also reduces hardware area necessary for interfaces, communication and control.

Shared bus architectures suffer from power and performance scalability limitations .Long bus wires are increasingly unfavourable in nanometre process technologies.

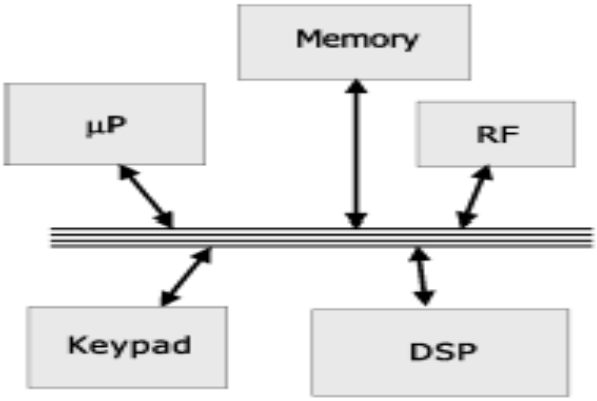


Fig (2). Bus Architecture.

D. Network on chip

The NoC architecture can overcome the long wire disadvantages from bus architectures, as on-chip switches are connected in a regular topology with point-to-point basis. The architecture is decoupled into transaction and physical layers.

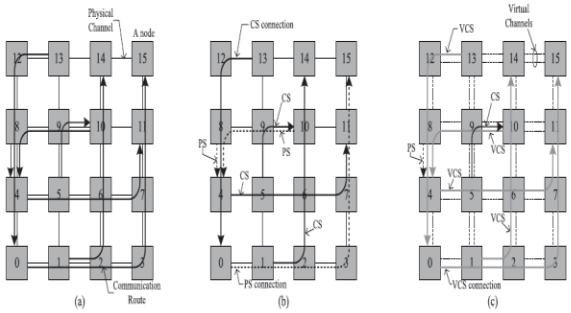
Thus the layered architecture enables independent optimization on both sides. With the Giga Transistor Chip era close at hand, the solution space of intra-chip communication is far from trivial.

NoC concept presents a possible unification of solutions for Electrical wires, System synchronization and design productivity. But in this Internal network contention may cause latency. Bus-oriented IPs needs smart wrappers.

Software needs clean synchronization in multiprocessor systems. System designers need re-education for new concepts. Network on Chip architecture

III. EXISTING SYSTEM

In Existing system a hybrid scheme for NOCs, which aims at obtaining low latency and low power consumption. In the presented hybrid scheme, a novel switching mechanism, called virtual circuit switching, is presented to intermingle with circuit switching and packet switching. Flits traveling in virtual circuit switching can traverse the router with only one stage. In addition, multiple virtual circuit-switched (VCS) connections are allowed to share a common physical channel. Moreover, a path allocation algorithm is presented in this paper to determine VCS connections and circuit-switched connections on a mesh-connected NoC, such thatboth communication latency and power are optimized. A set of synthetic and real traffic workloads are exploited to evaluate the effectiveness of this hybrid scheme.



Fig(3).hybrid scheme in a 4 × 4 mesh with 2VCs per input

A. Packet Switching (Store-and-Forward)

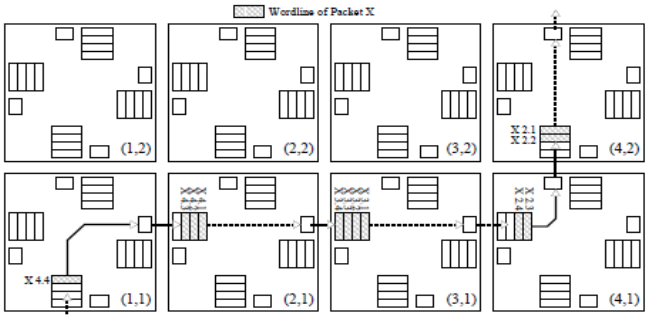


Fig (4) Store-and-Forward Switching.

Packet Switching method is commonly called also as Store-and-Forward (SAF) switching. This switching method is implemented by dividing data messages into a number of packets. Each packet is completely stored in a FIFO buffer before it is forwarded into the next router. Therefore, the size (depth) of FIFO buffers in the router is set similar to the size of the packet in order to be able to completely store the packet. Fig. shows the visual diagram of the store-and-forward switching method. As presented in the figure 4, message X consists of packets depicted with

Xn.m, where n is the packet number and m is the dataword (wordline) number in the packet. Each packet Xn.m as shown in the figure 4 consists of four wordlines. The first wordline (Xn.1) is the header and the last wordline(Xn.4) is the tail. The wordlines of the third packet for example, i.e. X3.1, X3.2, X3.3 andX3.4, are completely stored in the West input buffer of the router node (3,1). The packetX3.m can then be forwarded to the next router. If the routing has been made then the West input buffer of the router node (4,1) is free from data. The packet switching method is the first switching method that has been used in many parallel machines.

B. Virtual Cut-Through Switching

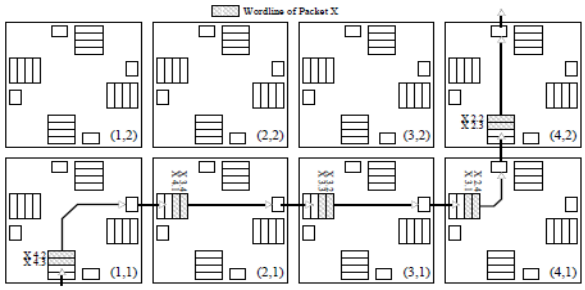


Fig.(5) Virtual Cut-Through Switching.

In the store-and-forward packet switching method, the packet is completely stored before it is forwarded to the next router. The delay to wait for the complete packet storing can be reduced by forwarding the first lines of the packet to the next router soon after routing has been made for the packet and when there is enough space in the required FIFO buffer in the next router to store the first wordlines of the packet. This switching technique is known as Virtual Cut-Through (VCT) switching and was firstly introduced in previous paper. On-chip router of Alpha 21364 is one of the multiprocessor system that uses VCT switching method. The visual diagram of the virtual cut-through switching method. As presented in the figure, the header of the third packet (X3.1) has been forwarded to the West input buffer in the router node (4,1), because routing has been made and there is already a free space to store the packet header. Meanwhile, the tail of the third packet(X3.4) is still behind in the West input buffer of the router node (2,1). The router in node(3,1) does not need to store the entire packet wordlines to forward the first wordlines of the packet. Hence, as shown in Fig, every packet can virtually cut-through in the network nodes.

C. Circuit Switching

The circuit switching method is commonly used in a connection-oriented communication protocol. The circuit switching method is performed by establishing connection and reserving some communication resources. When a virtual circuit from a source to a destination node has been configured and the successful connection has been informed by the destination node by sending a response packet to the source node, then the message can be transmitted through the network in a pipeline manner. At the end of the data transmission, a control packet is sent to the network to terminate the connection circuit. The circuit switching method is commonly used to provide guaranteed-bandwidth or guaranteed-throughput communication protocol for quality of service. The circuit switching method is originally used in telephone network

D.Limitations

The components such as five port router, crossbar switch increase the NoC area when compared with the conventional hybrid scheme in a 4 × 4 mesh-connected NoC Increasing of area leads more hardware as well as power & latency concern Physical channels are shared by more than one communication gives network traffic.
Area leads more hardware as well as power & latency concern.In order to support VCS, PS, and CS connections at the same time, a modified router architecture with five ports is proposed Compared with the baseline router the additional hardware of the proposed router includes the bypass path, the circuit configuration, and the VCS state.

IV. PROPOSED SYSTEM

Purpose of the present work is the integration of different bus-based systems with NoC-based approaches. From above discussion performances can be higher in NoC-based systems, but the simplicity and the presence of standards make bus-based systems more "usable". In this context, the proposed solution is driven by the effective requirements of interoperability of different communication domains; as a matter of fact, the increasing capabilities of modern digital devices makes it possible to integrate a huge amount of computational modules within a single chip.

This allows the definition of complex systems, in which there may exist multiple independent sub-systems, and it may be the case that these systems have to cooperate or at least exchange data information. This scenario is shown in which two different bus-based subsystems represent independent communication domains, in which different tasks can be performed. The shared NoC can make them communicate, in a transparent and flexible way. The inter-domain communication is provided by means of the Network-on-Chip protocol, and access to it is easily provided by the network interfaces (they are seen as IP-Cores on the bus).

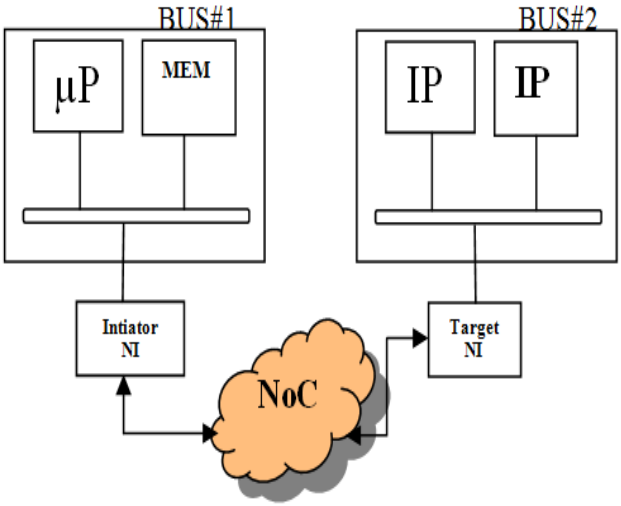


Fig (6). The integration of the NoC architecture with classical bus-based systems.

A. Classical bus based

In the proposed methodology NoC (Network on Chip) architecture for Classical Bus based systems to overcome the limitations of hybrid scheme by reducing switches and network interfaces. On chip communication architecture are classified into two type bus-based and network –based. The first group employ a sheared resource providing a centralized and controlled view of a physical channel

B. Classical design approaches

Classical design approaches are point-to-pinot and bus based architectures. This group employs a shared resource providing a centralised and controlled view of the physical channel.

C. Point-to-Point Architectures

In a point-to-point interconnect architecture, pairs of processing units communicate directly over dedicated physically wired connections Because of its simplicity, point-to-point interconnect has been widely adopted in many applications. Custom interconnect, sometimes referred as ad-hoc interconnect, and is simply connecting processing elements by wires when there is a necessity. On the other hand, uniform interconnect often has well defined interconnect topology.

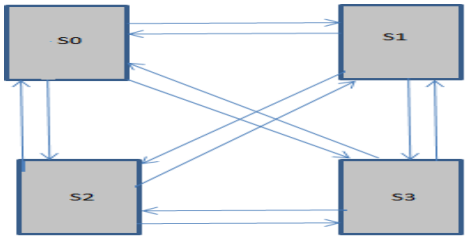


Fig (8). Point to point communication

D. Bus Based Architectures

The most relevant efforts to realize bus-based systems for reconfigurable architectures are BUS-COM and Reconfigurable Multiple Bus-on-Chip(RMBoC) . BUS-COM is divided into parallel channels as shown in Fig.9. Access to the shared medium is given by an arbiter, according to a static or dynamic slot assignment.

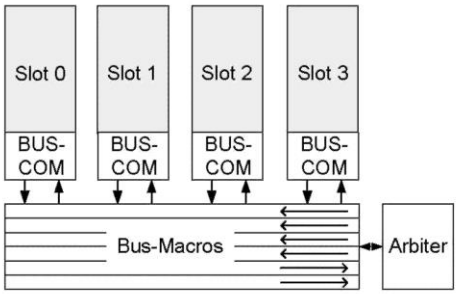
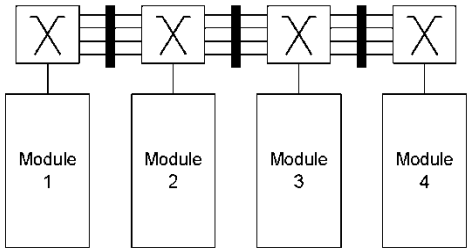


Fig (9).BUS-COM architecture.

RMBoC provides each computational module with a communication module, used to exchange information as shown in Fig 10.

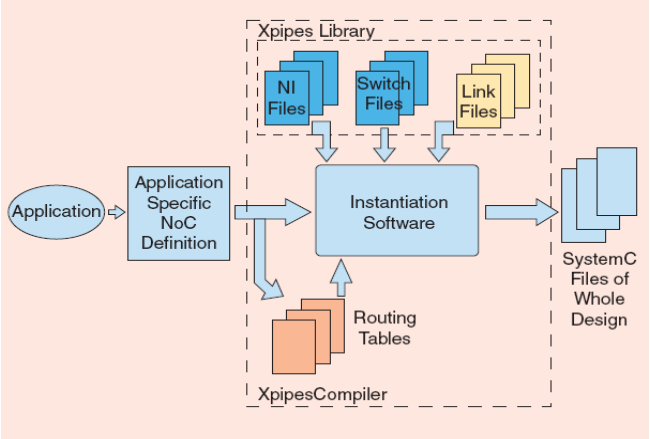


Fig(10). RMBoC architecture.

Both approaches lack flexibility and scalability due to the presence of a single physical channel. As a matter of fact, the increasing number of cores requires a major level of contention, and this may become soon unacceptable for high-performance embedded systems; in the worst case, a Denial-of-Service (DoS) would be reached. Flexibility is further limited by the static topology of the infrastructure, i.e. the logical path between each actor is defined once for all a priori, resulting in a much lower flexibility and adaptability to communication requirements.

E. Network-Based approaches

The implicit limitations previously described are overcome by the Network-on-Chip paradigm. The NoC approach However, they have also been applied in Systems-on-Chips (SoCs) architectures, as the connection scheme for different computational modules. The idea is to define a set of network elements, the switches, whose systematic interconnection implement the desired connectivity. To exploit full advantage of a scalable and flexible solution, packet-switching mechanism is used. Using a set of distributed elements ensures an implicit load balancing, resulting in a major level of flexibility, and a lower level of contention of the shared medium. XPipes is one of the first implementation of a Network-on-Chip approach, whose topology has to be defined at synthesis-time by enabling appropriate inter-switches communication links. Synthesis flow for NoC with Xpipes compiler is as shown in Fig 11



Fig(11). NoC synthesis flow with Xpipes compiler.

Xpipes limitation has been solved in CoNoChi(Configurable Network-on-Chip). Aim of CoNoChi is to support dynamic changes in the communication topology, adding (or removing) new (or existing) IP-Cores.

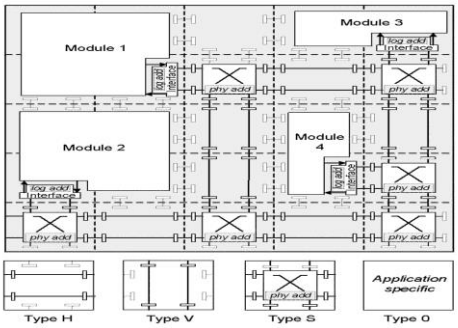


Fig (12).CoNoChi architecture.

F. Comparison b/w classical design and network based approaches

The two main design paradigms have their own advantages and disadvantages as reported since features from buses and NoCs can be used to design the desired infrastructure; it would be suitable to define an approach combining the advantages from both the domains. This is what the present work is based on.

G. Integration of NOC architecture with classical bus based system

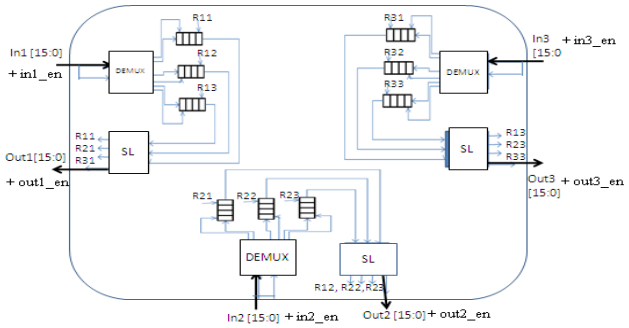


Fig (13) .Router Architecture

In order to support VCS, PS, and CS connections at the same time, a modified router architecture with five ports is Compared with the baseline router, the additional hardware of the presented router includes the bypass path, the circuit configuration, and the VCS state. First, the bypass path is added in each input unit for allowing flits to go directly to the crossbar switch. Second, each input unit contains a PS state and a VCS state. In this paper, both the PS and the VCS states have n fields corresponding to n VCs. In addition, these n VCs are shared by VCS

connections and PS connections. Information of the VCin the downstream router is stored in the VCS state to denote which downstream VC is connected to the corresponding VC. Incoming flits can directly traverse the crossbar switch according to the corresponding field of VCS state.

The VCS signal is used to preconfigure the crossbar switch for VCS connections. It can be transmitted simultaneously with the transmission offlits. The VCS signal is (log2 n + 1)-bit wide, including a VC identifier and a flag for representing its validity. The VCS signal does not traverse the crossbar switch, but is generated by the router. It is output when the crossbar switch just completes the configuration for the VCS connection during the SA stage. The overhead caused by VCS signal can be negligible. First, the VCS signal is only issued when crossbar switches of the VCS connection wait to be preconfigured. Due to the low activity of VCS signal, the power overhead caused by VCS signal can be much less than the power saving by bypassing buffer writing, routing, and arbitration of routers. Second, in the network with two VCs, the width of VCS signal is 2 bits .This chapter gives the brief explanation about the need of the integrated architecture, advantages and applications about the proposed On-chip Communication architecture.

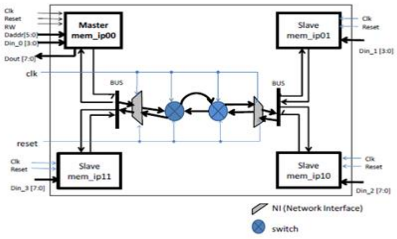
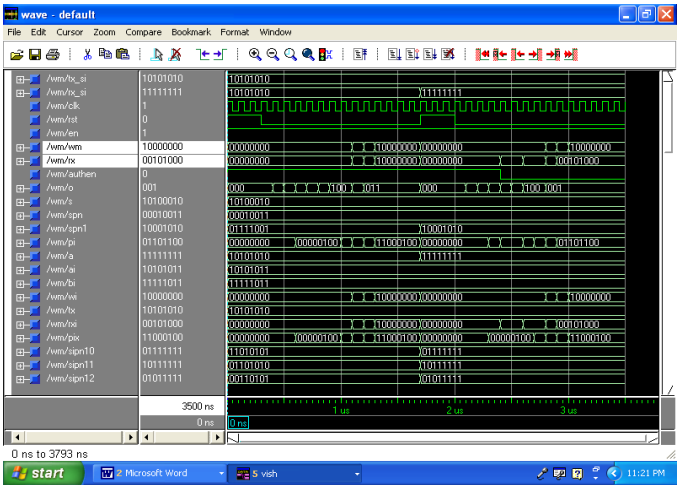


Fig (14) .Block diagram classical bus

V. VIEWING SIMULATION RESULT



To show the results of Unix shell simulation, Modelsim is invoked using
vsim -view <wlf_file> [-do <do-file.do>] .
Most times it is helpful to use a do-file similar to the do-file used for simulation. It should have the form
view wave
add wave <item_name>
add wave ...
....

VI. CONCLUSION

Network-on-Chip (NoC) architectures represent a promising design paradigm to cope with increasing communication requirements in digital systems. Network-on-chip (NoC) has emerged as a vital factor that determines the performance and power consumption of many-core systems. A novel switching mechanism, called virtual circuit switching, is implemented with circuit switching and packet switching. A path allocation algorithm is used to determine VCS connections and circuit-switched connections on a mesh-connected NoC, such that both communication latency and power are optimized. .VCS connections and CS connections can be limited to the class of communications that need guaranteed latency, and packet switching can be used to serve the best effort traffic slow power reduce router. HenceNOC architecture is design using classical bus based system in order to reduce power, area and reducing number of router.

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