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Design of SRAM Cell at Low Supply Voltage Based on Schmitt Trigger

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Abstract— Embedded SRAM is involved in many low-energy applications, e.g. stand-alone wireless sensor nodes. SRAMs have the highest energy contribution in such applications. Unlike dynamic RAM, it does not need to refresh. In modern Trends, the demand for memory has been increases tremendously. We analyze Schmitt-Trigger (ST)-based static random access memory (SRAM) bitcells for ultralow-voltage operation. The ST-based SRAM bitcells address the fundamental conflicting design requirement of the read versus write operation of a conventional 6T bitcell. The ST operation provides better read-stability as well as better write-ability compared to the standard 6T bitcell. This technology reduces power as well leakage current and improves signal noise margin (SNM).

Keywords— "SRAM, Schmitt-Trigger (ST), Stability, SNM, System-on-Chip(SoC), Low power"

I. INTRODUCTION

SRAM makes up a large portion of a system-on-chip (SoC) area, and most of the time, it also dominates the overall performance of a system. In addition to this, the tremendous growth in the popularity of mobile devices and other emerging applications, such as implanted medical instruments and wireless body sensing networks, necessitates the requirement of low-power SRAMs. Therefore, a strong low-power SRAM circuit design has drawn great research attention and has become significant [5]. However, a design of robust low-power SRAM faces many process and performance related challenges. This is because, in deep submicrometer technology, near subthreshold operation is very challenging due to increased device variations and reduced design margins. The conventional 6T SRAM cell suffers from read-current disturbance- induced SNM degradation with V_{dd} scaling. Moreover, due to increased variations at low supply voltages in advanced CMOS processes, caused by global and local process variations, the read stability and the write stability of 6T SRAM cell degrade to unacceptable level[4].

One of the major issues in the design of an SRAM cell is stability. The cell stability determines the sensitivity of the memory to process tolerances and operating conditions. It must maintain correct operation in the presence of noise signals. In particular, continued SRAM cell-area scaling for increased storage density, reduction in Supply voltage (V_{dd}) for lower stand-by power consumption, and enhanced yield necessary to realize larger-capacity SRAM arrays become increasingly difficult to achieve either by reducing the number of transistor use to design SRAM or by reducing the size of transistor.

Compared to Dynamic Random access memory (DRAM), SRAM does not have a capacitor to store the data, hence SRAM works without refreshing. In SRAM the data is lost when the memory is not electrically powered. Advances in chip design using CMOS technology have made possible the design of chips for higher integration, faster performance, and lower power consumption. To reach these objectives, the feature size of CMOS devices has been dramatically scaled to compact dimensions over the last few years. Power consumption of SRAMs account for a significant portion of the overall chip power consumption and due to high density, low power operation is a feature that has become a necessity in today's microprocessors. Various bit cells with varying number of transistors (6T–10T) have been proposed to solve the stability problem of the SRAM. In this project we scaled down the technology and variation of different parameter such as cell ratio (CR), voltage supply (Vdd), word line (WL) and bit line (BL). It has been most beneficial of performance of cell and size will reduce as much as possible.

II. CONVENTIONAL 6T SRAM CELL

The conventional 6T memory cell comprised of two CMOS invertors cross coupled with two pass transistors connected to a complimentary bit lines as shown in Fig. 1. The gate of access transistors N3 and N4 are connected to the WL (word line) to have data written to the memory cell or read from the memory cell through the BL or BLB (bitlines) during write and read operation[1].

The bit lines act as I/O buses which carry the data from the memory cell to the sense amplifier. Although it is not necessary to have two bit lines, both the signal and its inverse are typically provided in order to improve noise margins. SRAM cell perform three different operations, read, write and hold operation.

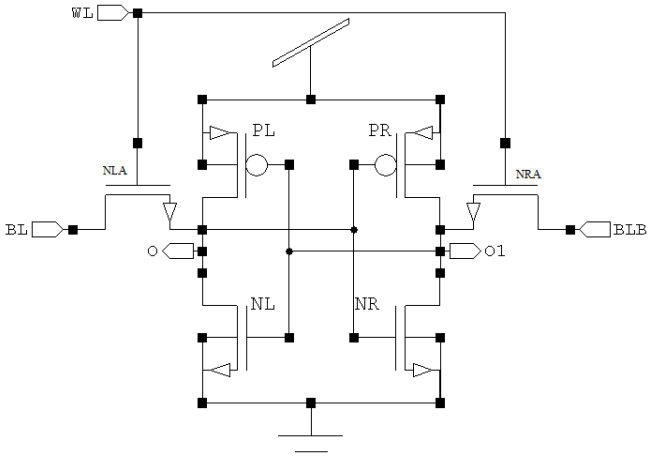

Fig. 1 Conventional 6T SRAM cell

III. STABILITY PROBLEM IN 6T SRAM CELL

The conventional 6T SRAM cell has the advantage of low static power consumption and very less area[5]. However, the main problem with the conventional 6T SRAM cell is shown in fig. 1 and the stability problem arising during the read operation, where the cell is most vulnerable towards noise and the stability of the cell is affected. The design of SRAM cell is essential for maintaining the correct operation. Therefore read static noise margin affects the cell stability. In order to avoid the problem of conventional 6T SRAM cell during read operation many new circuitry having different transistor count such as 6T,7T,8T,9T etc have been implemented. This causes the reduction in the read delay, speed of response of the cell and also increases the power consumption due to the increase in the transistor count. The need of battery operated device, the CMOS technology scaling continues.

IV. SCHMITT TIGGER BASED 11T SRAM

Single-ended SRAM topology is one of the very useful approaches for power-constrained applications. It reduces the leakage and switching power and also saves chip area. BLs have very high capacitance loading, particularly for sub-100-nm regime. During each read/write operation, the switching of BL costs significant dynamic power consumption. The single-ended scheme reduces one half of the active power for BL switching [3]. However, it incurs penalty in terms of increased read-/write-access time and degraded write '1' SNM at low supply voltages. This is the major limitation of a single-ended SRAM structure.

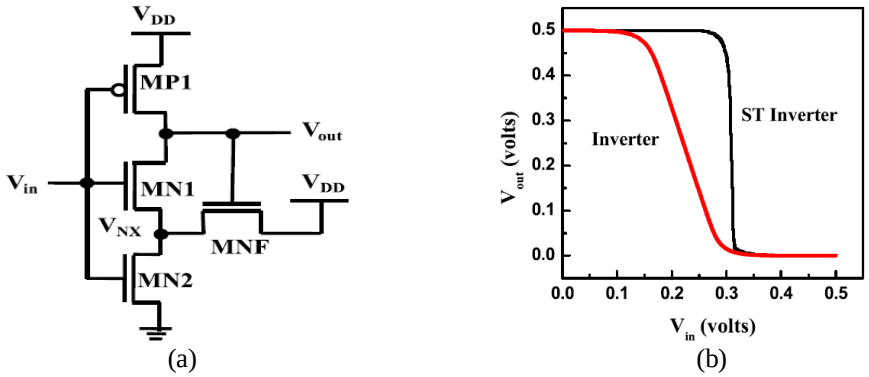

Fig. 2 (a) Basic ST inverter used for this design,
(b) Characteristics of inverter and ST inverter for 0 →1 transition at the input (V_{DD} =0.5V)[3]

Previously, Kulkarni *et al.* [4] proposed ST-based differential 10T SRAM cell (hereafter referred to as ST-1) with improved RSNM and robustness. Although the RSNM is increased as compared with the conventional 6T SRAM cell due to the inherent feedback mechanism of ST, this cell is still vulnerable to noise, since the 0 storing internal node of this cell rises to a voltage higher than ground during read operation (i.e., destructive read). Due to the voltage division between the cross-coupled ST and the access transistors, the stored data are disturbed, which is referred to as read upset [4].

In this work we present a single ended ST based 11T SRAM bitcell designed as shown in Fig. 3, that enhances data stability by improving the Read Static Noise Margin and also reduces the Power Consumption during read/write operation. The ST based 11T SRAM bicell consists of a cell core (cross-coupled ST inverter), a read path consisting of two access transistors, and a write-access transistor. The write-access transistor NLA is controlled by word line(WL), and the read-access transistor NRA2 is controlled by read WL (RWL). The feedback transistors of ST, NLF, and NRF are controlled by internal storage nodes O and O1, respectively, with their drains connected with V_{dd}.

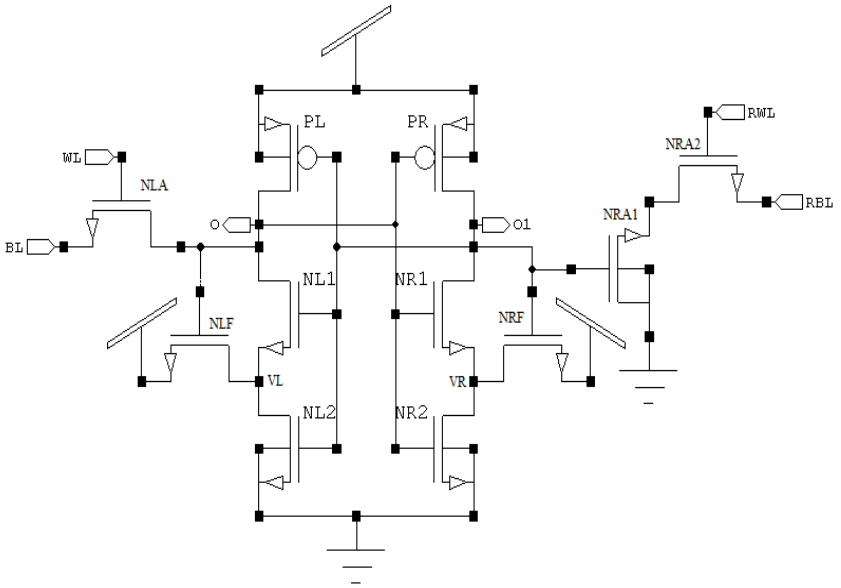

Fig. 3 Schmitt Trigger based 11T SRAM Bitcell

A. Hold Mode:

In the hold mode, both WL and RWL are disabled. Therefore, the cross-coupled ST inverter is isolated from both the BLs, and the data-holding capability is increased due to the feedback mechanism.

B. Read Mode:

During read operation, WL is disabled, whereas RWL is enabled, which provides discharging path for RBL through transistors NRA1 and NRA2 depending on the data stored at O1. The disabled WL makes data storage nodes (O and O1) decoupled from BL during the read access. Due to this isolation, the RSNM is almost the same as the HSNM. Since the HSNM is very high in ST-based cell, read stability is remarkably improved. The pull down transistors are at ground, so that storage node may not get disturbed during read operation. It is to be noted that in both read and hold mode, NLF and NRF are connected to V_{dd}, which helps the feedback

transistors NLF and NRF to provide a feedback mechanism and to exploit the feature of ST inverter to have a good inverter characteristic.

C. Write Mode:

For writing data into the cell, WL is activated to transfer the data to storage node from BL, which is set/reset according to the data to be written. RWL is disabled. Feedback transistors NLF and NRF are connected to supply voltage as the voltage at nodes VL and VR are high and it provides a feedback mechanism during write operation, but the writing speed is slightly decreased due to feedback mechanism. It improves the write ability of bitcell. The proposed bitcell employs read buffers to decouple storage nodes (O and O1) from BL to eliminate read-disturb problem along with the requirement of asymmetric write-assist mechanism for single-ended writing. Therefore, there is no transistor sizing conflict for read and write operations.

D. Application of Schmitt Trigger:

The Schmitt Trigger (ST) is a comparator that incorporates positive feedback. The circuit is named a "trigger" because the output retains its value until the input changes sufficiently to trigger a change. ST is used to modulate the switching threshold of an inverter depending on the direction of the input transition. The output state depends upon the input level and will change only as the input crosses a predefined circuit threshold. Therefore Schmitt Triggers are bistable networks that are widely used to enhance immunity of circuits to noise and disturbances [5]. The ST circuit has a dc transfer characteristic like an inverter, but with different switching thresholds depending on whether input signal is increasing or decreasing. ST can be used as a CMOS logic inverter. It has a number of applications in sub-threshold SRAM, frequency doublers, image sensors[8].

V. SIMULATION RESULTS

In this section, we extract various performance parameters of the proposed ST based SRAM cell like read stability or read SNM, hold SNM, read/write power, write ability etc. T-SPICE simulations were performed using 45-nm predictive technology model [PTM] to measure the figures of merit of an SRAM cell. In order to make a thorough comparison, we have compared our cell with 6T, ST-1[4]. A comparison of various performance metrics is presented in the following sub-sections.

A. Read Stability:

The read stability of an SRAM cell is determined in terms of RSNM. To find RSNM, Cell Ratio (CR) must be appropriately selected [2] as mentioned earlier. For Read Static Noise Margin, the word line and bit line is kept at high. Then the feedback between these two inverters is broken as shown in Fig. 4. By DC analysis, the voltage transfer characteristic (VTC) of the half cell is plotted between input and output voltage. This results butterfly curve by superimposing the VTC of one inverter to the inverse VTC of the other inverter of SRAM Cell [7].

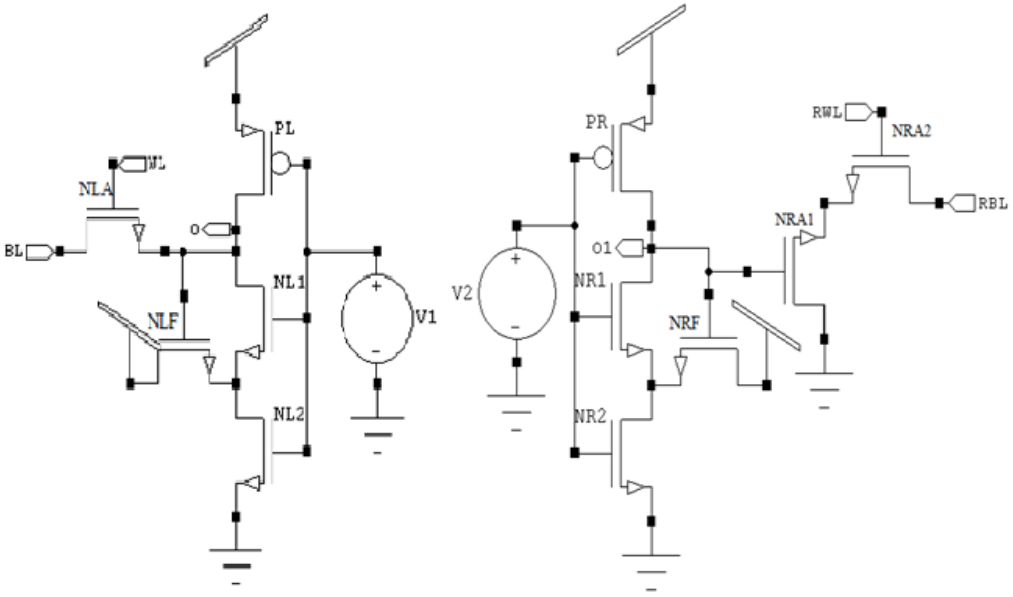

Fig. 4 ST-11T Read SNM schematic

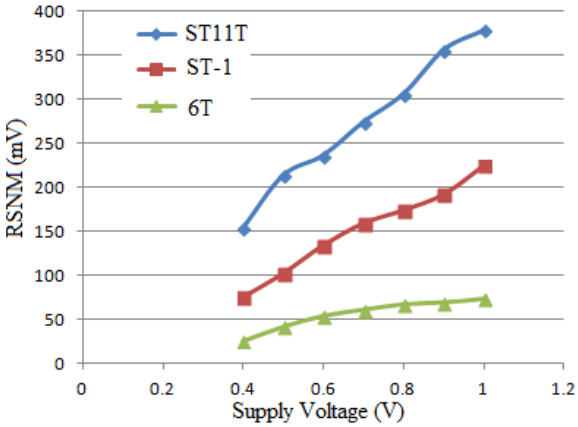

Fig. 5 Comparison of RSNM of different SRAM cells

B. Read/Write Power:

Fig. 6 shows the plot of read power of SRAM cells at different supply voltages. It is observed that 6T consume maximum power, while ST-1 consumes minimum read power.

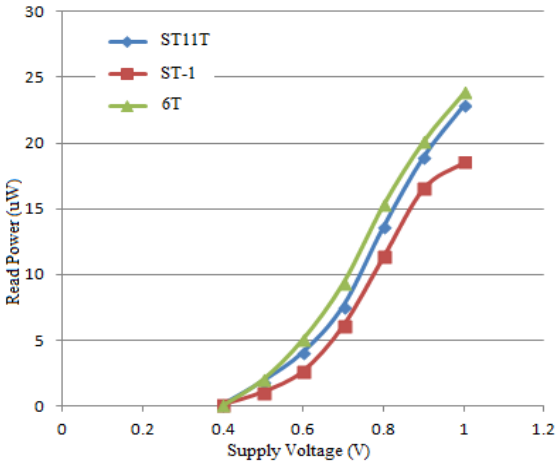

Fig. 6 Comparison of Read Power of SRAM cell

Table 1 shows the power consumption of the SRAM cells for write 0 and write 1 operation respectively. It is clear that the ST based 11T SRAM cell consumes least write 0 and write 1 power among all the considered cells.

Table 1
Write '1' and Write '0' Power at different supply voltages

Voltage (V)	**Write '1' Power (µW)**			**Write '0' Power (µW)**		
	ST-11T	**ST-1**	**6T**	**ST-11T**	**ST-1**	**6T**
0.4	0.02	0.14	0.11	0.02	0.14	0.11
0.5	2.13	2.21	2.65	2.13	2.21	2.65
0.6	4.29	4.58	4.71	4.29	4.58	4.71
0.7	7.01	7.16	7.59	7.01	7.16	7.59
0.8	10.23	13.56	15.22	10.23	13.56	15.22

0.9	15.49	18.42	21.92	15.49	18.42	21.92
1	19.20	21.09	24.83	19.20	21.09	24.83

C. Scalability:

Using predictive technology models (PTM), the ST based 11T bitcell is compared with the 6T cell to verify the effectiveness of our technique in scaled technologies [2]. The ST bitcell consistently predicts better read and hold SNM compared to the 6T cell in scaled technologies. For 32 nm technology, using predictive models, the ST bitcell predicts 1.6× improvement in read SNM compared to its 6T counterpart V_{dd} (400 mV) shown in Fig.7. For 90 nm technology, the ST based 11T bitcell predicts 1.58× improvement in read SNM compared to its 6T counterpart V_{dd} (400 mV) shown in Fig. 7. Thus, the proposed ST bitcell can be scalable into future technologies. As technology scales, with increased process variations, the memory cell failure probability would worsen at lower supply voltages. In such a scenario, the proposed ST bitcell with built-in feedback mechanism could be useful for low V_{dd} operation.

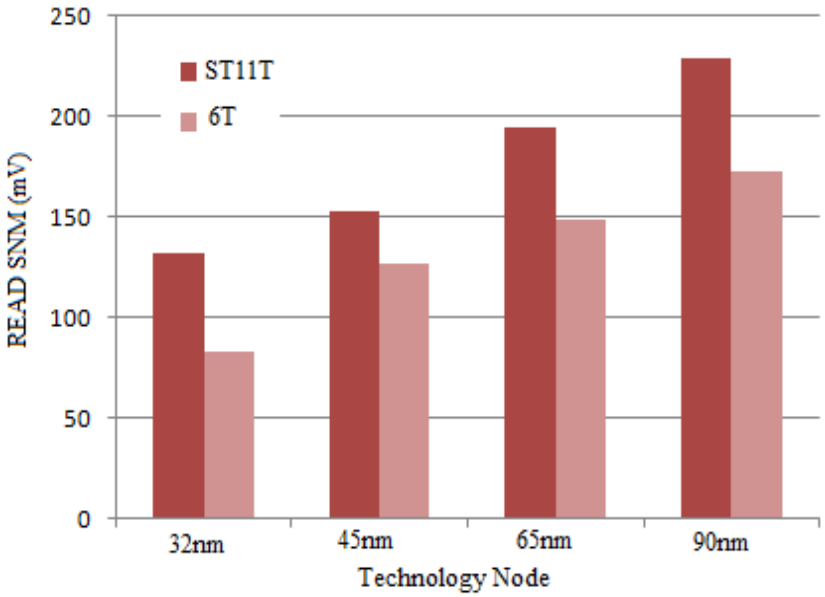

Fig. 7 Read SNM comparison for scaled technologies

VI. CONCLUSIONS

We presented a Schmitt trigger based single-ended, robust, 11-transistor SRAM bitcell suitable for subthreshold operation. The ST based 11T bitcell achieves higher read SNM (1.6×) compared to the conventional 6T cell (V_{dd} = 400 mV). The proposed cell significantly improved HSNM and RSNM while consuming least energy per operation among all the considered cells. We can say that power consumption in single ended is lesser than differential node SRAM. Read and write power is very less in single ended ST based SRAM. The presented cell achieved higher read noise margin at low supply voltages (0.4v-1v). The higher SNM can be achieved by modifying the device parameters of ST based 11T SRAM. However, the single-ended read and write operation in this cell affects read/write delay; nevertheless, the presented cell could be an agreeable choice for low-power applications where RSNM is of prime concern.

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