Available Online at www.ijcsmc.com

International Journal of Computer Science and Mobile Computing

A Monthly Journal of Computer Science and Information Technology

ISSN 2320–088X
IMPACT FACTOR: 6.017

IJCSMC, Vol. 6, Issue. 5, May 2017, pg.347 – 360

FAULT-TOLERANCE ROUTING IN 3-D NETWORK ON CHIP

SARITA SINGH
SHARDA UNIVERSITY
saritasingh0792@gmail.com

ABSTRACT: The increasing demand of numerous applications in consumer electronics has increased the number of computing resources in single chip. In such scenario, application needs many computing resources to build a System-on-Chip (SoC). Therefore, interconnection among Intellectual Property (IP) cores becomes another challenging issue. The execution of the system is measured regarding throughput. The throughput and effectiveness of interconnect relies on upon system parameters of the topology. Consequently, topology of any correspondence systems has a critical part to play for productive outline of system.

This works considers the outline of a productive tree-based topology to apply for Network-on-Chip. The level of proposed topology is 25% not as much as the torus alongside intense lessening in the width of proposed topology. We have gotten lessened degree for proposed topology that shifts from 3 to 6 for the system with k layers, while the measurement of topology is acquired as D= (2n-1) + k - 1. The introduced topology has adaptation to internal failure capacity to bolster the framework operation on account of connection disappointment. A substitute way has been given to accomplish blame tolerant topology. We have likewise displayed and reproduced an effective steering calculation that registers most limited way in the system.

I. INTRODUCTION

Due to growing demand of function in the electronics devices we need to accommodate many feature in the chip. And, this has given birth of a new dimension called System-on-Chip(SoC). System-On-Chip is to receive arrange like interconnections which is called Network-on-Chip (NoC) design. By applying system like correspondence which embeds a few switches in the middle of every correspondence question, the required wiring can be abbreviated. Along these lines, the switch-based interconnection instrument gives a great deal of adaptability and flexibility from the impediment of complex wiring. Substitution of SoC transports by NoCs offers high adaptability and the normality of a system structure, supporting less difficult interconnect demonstrating and more powerful circuits. The NoC likewise diminishes SoC fabricating cost, SoC time to advertise, SoC time to volume, and SoC configuration chance. The NoC approach has an unmistakable favorable position over conventional transports and most outstandingly framework throughput. The orders of crossbars or multilayered transports have qualities some place in the middle of conventional transports and NoC. We have demonstrated the contrast between a customary transport and Network-on-Chip.

Bus(Traditional Protocol)	**Network-on-chip(New Protocol)**
Bus uses simple protocol and is well understood.	Lightweight computer network protocols are applied to between the IP for communication.
The limited bandwidth is shared by all units attached to bus.	Total available bandwidth scales up with the network size.
The delay in bus arbiter grows with the number of masters.	The decision of routing and arbitration is distributed across the routers. Hence, delay remains constant.
The bus has only arbitration latency, other is almost zero.	Internal network contention has significant amount of latency.

II. RELATED WORK

Morteza Fathi, Sara Ebrahimi and Hossein Pedram [01], The phenomenal advance in semiconductor innovation has given awesome chances to popularized computationally serious applications. Amdahl's law was connected for multiprocessor PCs till quite a long while back yet his

laws are presently valuable to help us comprehend and create utilizing manycore chip multiprocessors (CMP). Clearly manycore-based plans wasn't possible blindfold and it needs point by point counts. In CMP's with hundred handling centers, 3D topology as system on-chip (NoC) can be utilized for shortening the wires length prompts to low dormancy, low power scattering and versatility. In the interim flaws can happen in NoC both at the switch and in communicational connections. There are many blame tolerant arrangements that their capacity depends on rerouting the parcels. In this paper we propose a blame tolerant method which is totally versatile and utilize accessible non-broken connections. The concentration of this procedure is keeping the execution of NoC when there is a flawed connection and the parcels from a source to a goal never get lost. Trial comes about demonstrates that this calculation can endure more than 10 defective connections in various parts of NoC and it can accomplish over 97% dependability.

Masoumeh Ebrahimi, Ronak Salamat, Nader Bagherzadeh, Masoud Daneshtalab [02], 3D NoC has its remarkable favorable circumstances more than 2D outline, for example, the littler impression and the shorter worldwide interconnects. Nonetheless, vertical interconnects are costly and inclined to flaws. It suggests that 3D NoCs may be meagerly associated. Such non-completely associated 3D NoCs require appropriate steering calculations to bolster the predetermined number of TSVs in the system where conventional calculations, for example, measurement arrange directing, XYZ, is not material any longer. In this paper, we propose a directing calculation for the meagerly associated 3D NoCs with one, two and one virtual channels along the X, Y and Z measurements, individually. This calculation is blame flexible, implying that it is working accurately for whatever length of time that there is no less than one TSV in the privilege most segment of the system.

Bouraoui Chemli and Abdelkrim Zitouni [03], Network on chip (NoC) is rising as another pattern for a Framework on chip (SoC) plan. The key focal points of NoC are superior and adaptability. In spite of those enhancements over the routine shared-transport based frameworks, NoC are not appeared as the perfect answer for the future SoC. As of late, with the three measurement (3D) innovation. The 3D NoC has been intended to beat the powerful utilization, high-cost correspondence and low throughput. This paper introduce a 3D switch outline which can bolster seven demands all the while. The customary Turn Display system utilized as a part of 2D NoC has been reached out on account of 3D NoC to keep away from gridlock clashes. Test brings about terms of zone, power and clock recurrence, generally to 2D NoC and others celebrated 3D switches has been examined.

Kavithra.B, Poovendran.R [04], NOC is the capacity to distinguish blame and disappointments in the engineering. It is adaptable and adaptable correspondence engineering. In this paper, we propose

discovery of information bundle and steering calculation mistakes. Both exhibited component is utilized to decide changeless and transient blunders and confine precisely the position of broken pieces in the switches, to saving throughput and information parcel inertness. The proposed strategy depends on new mistake recognition component reasonable for element NOCs, where the number and position of processor components change amid runtime. This paper gives the movement stack minor departure from normal idleness and power for DYAD steering calculation, this calculation having both deterministic and versatile directing calculation. This calculation is utilized to decide the way of a parcel from source to the goal. The best exhibitions of directing calculation in the NOC models are least idleness, least power and most extreme throughput. The point is to decrease the transmission delay and to guarantee the need to the most brief way directing of information. The reproduction result clarifies the viability of DYAD directing calculation under various movement designs**.**

Sudeep Pasricha, Yong Zou [05], Three dimensional incorporated circuits offer a critical chance to improve the execution of rising chip multiprocessors utilizing high thickness stacks gadget joining and shorter through silicon by means of interconnects that can lighten a portion of the issues connect with interconnect scaling in sub-65nm CMOS advancements. However Organize on-Chip textures that will associate the centers together in 3D-ICs will progressively be defenseless to perpetual and discontinuous issues, which can bring about disastrous framework disappointment. To beat these issues NoC Directing plan can be improved by including deficiency tolerant capacities, so they can adjust correspondence streams to take after blame free ways. Existing work has proposed different blame tolerant steering for 2D NoCs. In the paper surprisingly we explore blame tolerant directing plans in 3D NoCs. To accomplish high landing rates within the sight of flaws, we propose a novel low-overhead blame tolerant steering plan (4NP-First) for 3D NoCs. The proposed plan is appeared to have better versatility and adaptivity to deficiencies contrasted with existing measurement arrange, turn-show and stochastic arbitrary walk based 2D NoC Steering plan reached out to 3D NoCs.

Seyyed Hossein Seyyedaghaei Rezaei, Mehdi Modarressi, Reza Yazdani Aminabadi, Masoud Daneshtalab [06], The most imperative test in the rising 3D mix innovation is the higher temperature, especially in the layers that are more inaccessible from the warmth sink, contrasted with planar 2D chips. High temperature, thus, expands circuit's defenselessness to lasting and irregular issues. Then again, the quick and high-transmission capacity vertical connections in the 3D joining innovation have opened new skylines for system on-chip (NoC) outline advancements. In this paper, we use these ultra-low-inactivity vertical connections to outline a blame tolerant 3D NoC design. In this design, changeless and irregular imperfections on connections and crossbars are skirted by

acquiring the sit still data transmission from vertically adjoining connections and crossbars. Assessment comes about under engineered and practical workloads demonstrate that the proposed adaptation to internal failure system offers higher unwavering quality and lower execution misfortune, when contrasted and cutting edge blame tolerant 3D NoC plans.

Abdulaziz Alhussien, Freek Verbeek, Bernard van Gastel, Nader Bagherzadeh and Julien Schmaltz [07], A fault-tolerant versatile wormhole steering capacity for Systems on-Chips (NoCs) is exhibited. The oddity of this directing rationale is that it is equipped for utilizing runtime data on accessibility of connections to progressively sidestep broken channels. At the point when deficiencies happen, no disconnected reconfiguration or dropping of bundles is vital. Rather, dynamic courses are recommended on-the-fly. Steering choices are construct just with respect to nearby information, which takes into consideration quick exchanging. Our approach does not utilize any exorbitant virtual channels. As we don't restrict cyclic conditions, the steering capacity gives insignificant directing from source to goal even within the sight of shortcomings. We have executed the engineering configuration utilizing synthesizable HDL. Utilizing reenactments, we have evaluated the overhead of our approach as far as inertness, power and region. All things considered, even with 40% of the connections broken our steering rationale is competent performing accurately. Utilizing formal check, we have demonstrated 100% dependability up to three issues, i.e., for any blend of three blames our directing rationale stays associated, gridlock free and sans livelock.

Kavithra.B, Poovendran.R [08], NOC is the capacity to distinguish blame and disappointments in the design. It is adaptable and adaptable correspondence design. In this paper, we propose identification of information bundle and directing calculation mistakes. Both introduced instrument is utilized to decide lasting and transient blunders and restrict precisely the position of flawed pieces in the switches, to safeguarding throughput and information parcel inactivity. The proposed strategy depends on new mistake identification component appropriate for element NOCs, where the number and position of processor components fluctuate amid runtime. This paper gives the movement stack minor departure from normal dormancy and power for DYAD steering calculation, this calculation having both deterministic and versatile directing calculation. This calculation is utilized to decide the way of a bundle from source to the goal. The best exhibitions of steering calculation in the NOC designs are least idleness, least power and most extreme throughput. The point is to lessen the transmission delay and to guarantee the need to the most limited way directing of information. The recreation result clarifies the viability of DYAD directing calculation under various activity designs.

Ashkan Eghbal, Student Member, IEEE, Pooria M. Yaghini, Student Member, IEEE, Nader Bagherzadeh, Fellow, IEEE, and Misagh Khayyambashi [09], Reliability is a standout amongst the most difficult issues with regards to Three-Dimensional System on-Chip (3D NoC) frameworks. Unwavering quality investigation is conspicuous for early phases of the assembling procedure keeping in mind the end goal to avert exorbitant updates of an objective framework. This article classifies the potential physical flaws of a standard TSV-based 3D NoC engineering by focusing on Two-Dimensional (2D) NoC parts and their between kick the bucket associations. In this paper, Through-Silicon By means of (TSV) issues, warm concerns, and Single Occasion Impact (SEE) are examined and arranged, keeping in mind the end goal to propose assessment measurements for reviewing the versatility of 3D NoC outlines. An unwavering quality examination for significant wellspring of flaws is accounted for in this article independently in light of their Interim to Disappointment (MTTF). TSV disappointment likelihood instigated by inductive and capacitive coupling is likewise talked about. At last, the paper gives a formal dependability investigation on the totaled deficiencies that influence TSV. This formal examination is basic for evaluating the flexibility of various segments with a specific end goal to relieve the repetition cost of blame tolerant outline or to look at the efficiency of any proposed blame tolerant strategies for 3D NoC structures.

Siavoosh Payandeh Azad, Behrad Niazmand, Jaan Raik, Gert Jervan, Thomas Hollstein [10], In this paper we describe a holistic approach for Fault-Tolerant Network-on-Chip (NoC) based many-core systems that incorporates a System Health Monitoring Unit (SHMU) which collects all the fault information from the system, classifies them and provides different solutions for different fault classes. A Mapper/Scheduler Unit (MSU) is used for online generation of different mapping and scheduling solutions based on the current fault configuration of the system. For detection of faults, we have leveraged concurrent online checkers, able to capture faults with low detection latency and providing the fault information for SHMU, which can be later used for the recovery process. The experimentation setup is performed in an open source tool, able to perform the mapping, scheduling and simulation of the system.

Michael Opoku Agyeman [11], Recently three-dimensional Networks-on-Chips (3D NoCs) ranging from regular to highly irregular topologies have been realized as efforts to improve the performance of applications in both general purpose and application-specific multi-core domain. However, faults can cause high contentions in NoCs. As a solution, adaptive routing algorithms are used. On the other hand, these algorithms have high area and timing overheads due to extra logic required for adaptively. We present a novel fault reporting scheme as well as a fault-tolerant routing algorithm for

emerging 3D NoCs. The proposed algorithm analyses the condition of the NoC resources and distance of the destination nodes to reroute packets. The algorithm has been evaluated by synthetic and various real-world traffic patterns. Experimental results show that the proposed algorithm has significant reduction in packet delays (over 45%) compared to other algorithms.

Chaochao Feng, Minxuan Zhang, Zhonghai Lu, Axel Jantsch [12], This paper proposes a low-overhead fault-tolerant deflection routing algorithm, which uses a layer routing table and two TSV state vectors to make efficient routing decision to avoid both TSV and horizontal link faults, for 3D NoC. The proposed switch is implemented in hardware with TSMC 65nm technology, which can achieve 250MHz. Compared with a reinforcement-learning-based fault-tolerant deflection switch with a global routing table, the proposed switch occupies 40% less area and consumes 49% less power consumption. Simulation results demonstrate that the proposed switch has 5% less average packet latency than the switch with the global routing table under real application workloads and with only 5% performance degradation under synthetic workloads in the presence of 10% link faults.

Chaoyun Yao , Chaochao Feng , Minxuan Zhang , Wei Guo , Shouzhong Zhu1, and Shaojun Wei [13], In this paper, we proposed two region partition multicast routing algorithms for the 3D mesh Interconnection Network to enhance the overall system performance. The proposed two algorithms shorten the network long path latency. Compared to the based multicast routing algorithm, our simulations with six different synthetic workloads reveal that our architecture acquires high system performance.

AWET YEMANE WELDEZION [14], Three-Dimensional (3D) integration of circuits based on die and wafer stacking using through-silicon-via is a critical technology in enabling "more- than-Moore", i.e. functional integration of devices beyond pure scaling ("more Moore"). In particular, the scaling from multi-core to many-core architecture is an excellent candidate for such integration. Nevertheless, as much as there are opportunities to explore, designing systems using 3D integration technology has many challenges to tackle. It follows a complex design process involving integration of heterogeneous technologies. It is also expensive to prototype because the 3D industrial ecosystem is not yet complete and ready for low-cost mass production.

With trends leading towards 3D many-core architecture, it is also imperative to extend the under-lying Networks-on-Chip (NoC) to efficiently facilitate the communication of such massively integrated cores on a 3D chip. In this thesis scalability and performance issues of NoCs are explored in terms of architecture, organization and functionality of many-core systems. The key contributions of the thesis are made by (1) addressing the challenges in modeling and development of deflection routing NoCs for the use in regular and irregular networks, (2) evaluating new configurations of 3D processor-memory stacking, (3) the use of multi-rate vertical interconnect to optimize network performance, and (4) developing predictive models for performance analysis in many-core architecture.

Mostefa BELARBI [15], The suggested new approach based on B-Event formal technics consists of suggesting aspects and constraints related to the reliability of NoC (Network-On-chip) and the over-cost related to the solutions of tolerances on the faults: a design of NoC tolerating on the faults for SoC (System-on-Chip) containing configurable technology FPGA (Field Programmable Gates Array), by extracting the properties of the NoC architecture. We illustrate our methodology by developing several refinements which produce QNoC (Quality of Service of Network on chip) switch architecture from specification to test. We will show how B-event formalism can follow life cycle of NoC design and test: for example the code VHDL (VHSIC Hardware Description Language) simulation established of certain kind of architecture can help us to optimize the architecture and produce new architecture; we can inject the new properties related to the new QNoC architecture into formal B-event specification. B-event is associated to Rodin tool environment. As case study, the last stage of refinement used a wireless network in order to generate complete test environment of the studied application.

III. PROBLEM STATEMENT

The dissertation work will carry out investigation/survey on topology and routing with primary focus on 3-D Network-on-Chip. The investigation consists of a detailed exploration by means of the theoretical proofs, simulation and analysis. The routing strategy in 3-D considers routing at every layer apart from via interconnects. We will propose a new topology and routing algorithm for 3-D Network-on-Chip that would reduce the costs (network degree x diameter, latency). We will explore irregular tree based 3-D topologies.

IV. PROPOSED METHOD

Most important thing in the NoC design is its topology androuting algorithm. Sending packets from Source node (S) to the Destination node (D) efficiently from various available paths without any congestion or fault with low cost is the main goal of the routing algorithm.

Approach to Reduce the Network Cost:

We will design a new topology which will have some basic module as shown below. The structure contains only three nodes. Every node in the basic module is capable to communicate to other nodes directly without any hop. Thus, diameter of the basic module is only 1. In the below figure we have shown a tree with of level 2 and 3 also. The level is formed by extending terminal nodes.

Now, we need to derive the network parameters for the proposed tree. We will find out derivation for followings:

- Total number of nodes (N)
- Average degree (d)
- Diameter of the network (D)

V. IMPORTANT ALGORITHMS

Routing:

- Routing is the way toward choosing ways in a system along which to send arrange movement.

- Goals of directing are accuracy, effortlessness, Strength, Dependability, Decency and Optimality.
- Routing is performed for some sorts of system, including the phone organize, electronic information systems and transportation systems.
- Routing Algorithms can be classified based on the following:

1. Static or Dynamic Routing,
2. Distributed or Centralized,
3. Single path or Multi path,
4. Flat or Hierarchical,
5. Intra Domain or Inter Domain,
6. link State or Distance Vector.

- Algorithms might be static, the steering choices are set aside a few minutes, with data about the system topology and limit, then stacked into the switches.
- Algorithms might be progressive, where the switches settle on choices in light of data they assemble, and the courses change after some time, adaptively.
- Routing can be assembled into two classes: Non-versatile steering , and Versatile directing.
- **Non-adaptive Routing**
- Once the pathway to goal has been chosen, the switch sends all bundles for that goal along that one course.
- The directing choices are not made in light of the condition or topology of the system.
- Examples: Brought together, Confined, and Dispersed Calculations

Adaptive Routing

- A switch may choose another course for every parcel (even bundles having a place with a similar transmission) because of changes in condition and topology of the systems.
- Examples: Flooding, and Arbitrary Walk.

Routing Algorithms

Shortest Path Routing:

Links between switches have a cost related with them. As a rule it could be a component of separation, data transfer capacity, normal activity, correspondence cost, mean line length, measured postponement, switch preparing speed, and so forth.

The briefest way calculation just finds the slightest costly way through the system, in view of the cost work.

Examples: Dijkstra's algorithm

Distance Vector Routing:

In this routing scheme, each router periodically shares its knowledge about the entire network with its neighbours.

Every switch has a table with data about system. These tables are refreshed by trading data with the quick neighbors.

It is otherwise called Belman-Passage or Portage Fulkerson Calculation.

It is utilized as a part of the first ARPANET, and in the Web as Tear.

Neighboring hubs in the subnet trade their tables occasionally to refresh each other on the condition of the subnet (which makes this a dynamic calculation). On the off chance that a neighbor cases to have a way to a hub which is shorter than your way, you begin utilizing that neighbor as the course to that hub.

Separate vector conventions (a vector contains both separation and bearing, for example, Tear, decide the way to remote systems utilizing jump consider the metric. A jump consider is characterized the quantity of times a bundle needs to go through a switch to achieve a remote goal.

For IP Tear, the most extreme bounce is 15. A bounce number of 16 demonstrates an inaccessible system. Two forms of Tear exist: rendition 1 and variant 2.

IGRP is another case of a separation vector convention with a higher bounce check of 255 jumps.

Intermittent updates are sent at a set interim. For IP Tear, this interim is 30 seconds.

Updates are sent to the communicate address 255.255.255.255. Just gadgets running directing calculations tune in to these updates.

At the point when a refresh is sent, the whole steering table is sent.

Link State Routing:

The accompanying arrangement of steps can be executed in the Connection State Steering.

The premise of this promoting is a short stuffed called a Connection State Bundle (LSP).

OSPF (Open briefest way first) and IS-IS are cases of Connection state steering.

Interface State Packet(LSP) contains the accompanying data:

The ID of the hub that made the LSP;

A rundown of straightforwardly associated neighbors of that hub, with the cost of the connection to every one;

A succession number;

An opportunity to live(TTL) for this parcel.

At the point when a switch surges the system with data about its neighborhood, it is said to promote.

Find your neighbors

Measure deferral to your neighbors Package all the data about your neighbors together Send this data to every single other switch in the subnet

Process the most limited way to each switch with the data you get

Every switch discovers its own most limited ways to alternate switches by utilizing Dijkstra's calculation.

In connection state directing, every switch imparts its information of its neighborhood to all switches in the system.

Connect state conventions execute a calculation called the most limited way first (SPF, otherwise called Dijkstra's Calculation) to decide the way to a remote goal.

There is no bounce tally confine. (For an IP datagram, the most extreme time to live guarantees that circles are dodged.)

Just when changes happen, It sends all outline data like clockwork as a matter of course. Just gadgets running directing calculations tune ito these updates. Updates are sent to a multicast address.

Updates are speedier and union circumstances are decreased. Higher CPU and memory necessities to keep up connection state databases.

Connect state conventions keep up three separate tables:

Neighbor table: It contains a rundown of all neighbors, and the interface each neighbor is associated off of. Neighbors are framed by sending Hi bundles.

Topology table (Connection State table) : It contains a guide of all connections inside a zone, including each connection's status.

Steering table: It contains the best courses to every specific goal

Flooding Algorithm:

It is a non-adaptive algorithm or static algorithm.

At the point when a switch gets a parcel, it sends a duplicate of the bundle out on each line (aside from the one on which it arrived).

To forestall frame circling perpetually, every switch decrements a bounce include contained the bundle header.

When the bounce check decrements to zero, the switch disposes of the bundle.

Flow Based Routing Algorithm:

It is a non-adaptive routing algorithm.

It considers both the topology and the heap in this steering calculation;

We can gauge the stream between all sets of switches.

From the known normal measure of movement and the normal length of a parcel you can register the mean bundle defers utilizing lining hypothesis.

Stream based steering then tries to discover a directing table to limit the normal parcel delay through the subnet.

Given the line limit and the stream, we can decide the deferral.

REFERENCES

[01] Morteza Fathi, Sara Ebrahimi and Hossein Pedram, **"A fault-tolerant routing algorithm in 3D topology many core processors",** Journal of Informatics and Computer Engineering (JICE) Vol. 1(1), Oct. 2015, pp. 04-09, JICE DOI: 649123/10.112551,

[02] Masoumeh Ebrahimi, Ronak Salamat, Nader Bagherzadeh, Masoud Daneshtalab, **"A Fault Resilient Routing Algorithm for Sparsely Connected 3D NoCs",** 2015 4th MEDIAN Workshop,

[03] Bouraoui Chemli and Abdelkrim Zitouni**,"A Turn Model Based Router Design for 3D Network on Chip",** World Applied Sciences Journal 32 (8): 1499-1505, 2014, ISSN 1818-4952, DOI: 10.5829/idosi.wasj.2014.32.08.1254,

[04] Kavithra.B, Poovendran.R, **"Fault Detection and DyAD Algorithm for NOC Architecture",** International Journal of Innovative Research in Science, Engineering and Technology, Volume 5, Special Issue 2, March 2016, ISSN (Online): 2319 – 8753, ISSN (Print) : 2347 – 6710,

[05] Sudeep Pasricha, Yong Zou, **"A Low Overhead Fault tolerant Routing Scheme for 3D network-on-Chip",** 978-1-61284-914-0/11/$26.00 @2011 IEEE,

[06] Seyyed Hossein Seyyedaghaei Rezaei, Mehdi Modarressi, Reza Yazdani Aminabadi, Masoud Daneshtalab, **"Fault-Tolerant 3-D Network-on-Chip Design using Dynamic Link Sharing",** 978-3-9815370-7-9/DATE16/ @2016 EDAA,

[07] Abdulaziz Alhussien, Freek Verbeek, Bernard van Gastel, Nader Bagherzadeh and Julien Schmaltz**, "Fully Reliable Dynamic Routing Logic for a Fault-Tolerant NoC Architecture",** Journal of Integrated Circuits and Systems 2013; v.8 / n.1:43-53,

[08] Kavithra.B, Poovendran.R , **"Efficient Fault Detection and Dyad Routing Algorithm for 3D Network on Chip",** International Journal of Innovative Research in Computer and Communication Engineering, Vol. 4, Issue 3, March 2016, ISSN(Online): 2320-9801, ISSN (Print) : 2320-9798,

[09] Ashkan Eghbal, Student Member, IEEE, Pooria M. Yaghini, Student Member, IEEE, Nader Bagherzadeh, Fellow, IEEE, and Misagh Khayyambashi, **"Analytical Fault Tolerance Assessment and Metrics for TSV-based 3D Network-on-Chip",** Department of Electrical Engineering and Computer Science, University of California, Irvine, CA, 92697 USA,

[10] Siavoosh Payandeh Azad, Behrad Niazmand, Jaan Raik, Gert Jervan, Thomas Hollstein, **"Holistic Approach for Fault-Tolerant Network-on-Chip based Many-Core Systems",** arXiv:1601.07089v1 [cs.DC] 26 Jan 2016,

[11] Michael Opoku Agyeman, **"A Low Overhead Fault Reporting Scheme for Resilient 3D Network-on-Chip Applications",** Communications on Applied Electronics (CAE) - ISSN : 2394-4714, Volume 2 - No. 4, July 2015,

[12] Chaochao Feng, Minxuan Zhang, Zhonghai Lu, Axel Jantsch, **"A Low-overhead Fault-aware Deflection Routing Algorithm for 3D Network-on-Chip",** National Natural Science Foundation of China under Grant No. 60970036, No. 60873212 and No. 61003301,

[13] Chaoyun Yao , Chaochao Feng , Minxuan Zhang , Wei Guo , Shouzhong Zhu1, and Shaojun Wei, **"Partitioning Methods for Multicast in Bufferless 3D Network on Chip",** Springer-Verlag Berlin Heidelberg 2016, W. Xu et al. (Eds.): NCCET 2015, CCIS 592, pp. 13–22, 2016, DOI: 10.1007/978-3-662-49283-3 2,

[14] AWET YEMANE WELDEZION, **"Exploring the Scalability and Performance of Networks-on-Chip with Deflection Routing in 3D Many-core Architecture",** KTH School of Information and Communication Technology, SE-164 40 Kista, Sweden, TRITA-ICT 2015-29, ISBN 978-91-7595-803-3,

[15] Mostefa BELARBI, **"Formal and Informal Modeling of Fault Tolerant Noc Architectures"** , I.J. Intelligent Systems and Applications, 2015, 12, 32-42, DOI: 10.5815/ijisa.2015.12.03,

