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RESEARCH ARTICLE

Study of Outpouring Power Diminution Technique in CMOS Circuits

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Abstract- The most research on the power consumption of circuits has been concentrated on the switching power and the power dissipated by the leakage current has been relatively minor area. In today's IC design, one of the key challenges is the increase in power dissipation of the circuit which in turn shortens the service time of battery powered electronics, reduces the long term reliability of circuits due to temperature induced accelerated device and interconnects aging processes, and increases the cooling and packaging costs of these circuits. In this paper the main aim is to reduce power dissipation. In this paper we use GALEOR (Gated Leakage transistOR) technique to reduce the leakage power. The advantage with GALEOR compared to other leakage reduction techniques is not affecting the dynamic power. Further, the proposed technique overcomes the limitations posed by other existing methods for leakage reduction.

Keywords: Subthreshold Leakage, Gate Oxide Tunneling, Leakage Current, LECTOR, GALEOR

I. INTRODUCTION

Power dissipation is an important consideration in the design of CMOS VLSI circuits. High power consumption leads to reduction in the battery life in the case of battery-powered applications and affects reliability, packaging, and cooling costs. The short-circuit power dissipation can be reduced to 10% of total power dissipation by designing the circuit to have equal input and output rise/fall edge times. The power dissipation resulting from switching activity is the dominant component for technology processes with feature size larger than 1 m.With technology processes maturing toward the deep-submicron regime, the feature sizes of the transistors are becoming smaller, thereby reducing the load capacitance. The reduction in feature size also forces a reduction in the supply voltage. The voltage scaling technique takes benefit of the quadratic dependence of switching power on supply voltage for dynamic power savings. However, this technique pays a penalty for the operation of the circuit by increasing the delay drastically as supply voltage approaches the threshold voltage of the devices. In order to facilitate voltage scaling without affecting the performance, threshold voltage has to be reduced.

In general, the ratio between the supply voltage and the threshold voltage should be at least 5, so that the performance of CMOS circuits is not affected. This also leads to better noise margins and helps to avoid the hot-carrier effects in short-channel devices.

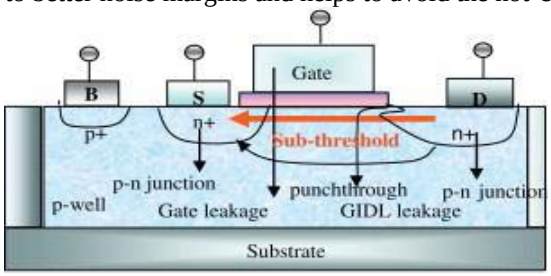

Fig1.1: Static CMOS leakage sources.

Leakage power of a CMOS transistor depends on gate length and oxide thickness. To decrease the dynamic power, the supply voltage is decreased which leads to the performance degradation. To speed up the device, the threshold voltage should also be scaled down along with the supply voltage, which results in exponential increase in the sub-threshold leakage current, thereby increase in the static power dissipation. The main components of leakage current in a MOS transistor are shown in Figure 1.1.Scaling down of threshold voltage results in exponential increase of the sub threshold leakage current. The supply voltage and threshold voltage scaling trends for Intel's microprocessor process technologies are discussed. It can be seen from that the leakage power is only 0.01% of the active power for 1- m technology, while it is 10% of the active power for 0.1- m technology. There is a fivefold increase in leakage power as the technology process advances to a new generation. Projecting these trends, it can be seen that the leakage power dissipation will equal the active power dissipation within a few generations. Hence, efficient leakage power reduction methods are very critical for the deep-submicron and nanometer circuits.

II. TRANSISTOR LEAKAGE MECHANISMS

A. Sub-threshold leakage current (I_{sub})

MOS transistors occur when the gate voltage is below the threshold voltage and mainly consists of diffusion current. Off-state leakage in present-day devices is usually dominated by this type of leakage. An effect called drain-induced barrier lowering (DIBL) takes place when a high-drain voltage is applied to a short channel device. The source injects carriers into the channel surface (independent of gate voltage). Narrow width of the transistor can also modulate the threshold voltage and the sub-threshold current.

$$I_o = \mu_0 C_{ox} \frac{W}{L_{eff}} \left(\frac{kT}{q}\right)^2 e^{1.8} e^{\frac{q\delta V_t}{\eta kT}} \quad (1.1)$$

Where, μ0 is the zero bias mobility, Cox is the gate oxide capacitance, and (W/L) represents the width to the length ratio of the leaking MOS device. The variable V in equation 1.1 is the thermal voltage constant, and V_{gs} represents the gate to the source voltage. The parameter n in equation is the sub-threshold swing coefficient given by $1 + (C_d/C_{ox})$ with C_d being the depletion layer capacitance of the source/drain junction. One important point about equation 1.1 is that the sub threshold leakage current is exponentially proportional to (Vgs-Vth). Shorter channel length results in lower threshold voltages and increases sub-threshold leakage. As temperature increases, sub-threshold leakage is also increased. On the other hand, when the well-to-source junction of a MOSFET is reverse biased, there is a body effect that increases the thresh-old voltage and decreases sub-threshold leakage.

B.Gate oxide tunneling current (I_{gate})

Tunneling of electrons that can result in leakage when there is a high electric field across a thin gate oxide layer. Electrons may tunnel into the conduction band of the oxide layer; this is called Fowler- Nordheim tunneling. In oxide layers less than 3-4 nm thick, there can also be direct tunneling through the silicon oxide layer. Mechanisms for direct tunneling include electron tunneling in the conduction band, electron tunneling in the valence band, and hole tunneling in the valence band.

C. Junction leakage

That results from minority carrier diffusion and drift near the edge of depletion regions, and also from generation of electron hole pairs in the depletion regions of reverse-bias junctions. When both n regions and p regions are heavily doped, as is the case for some advanced MOSFETs, there is also junction leakage due to band-to-band tunneling (BTBT).

D. Hot-carrier injection

It occurs in short-channel transistors. Because of a strong electric field near the silicon/silicon oxide interface, electrons or holes can gain enough energy to cross the interface and enter the oxide layer. Injection of electrons is more likely to occur, since they have a lower effective mass and barrier height than holes.

E. Gate-induced drain leakage (GIDL)

This is caused by high field effect in the drain junction of MOS transistors. In a negative- channel metal-oxide-semiconductor (NMOS) transistor, when the gate is biased to form accumulation layer in the silicon surface under the gate, the silicon surface has almost the same potential as the p-type substrate, and the surface acts like a p region more heavily doped than the substrate. When the gate is at zero or negative voltage and the drain is at the supply voltage level, there can be a dramatic increase of effects like avalanche multiplication and band-to-band tunneling. Minority carriers underneath the gate are swept to the substrate, completing the GIDL path.

F. Punch through leakage

This occurs when there is decreased separation between depletion regions at the drain-substrate and the source-substrate junctions. This occurs in short-channel devices, where this separation is relatively small. Increased reverse bias across the junctions further decreases the separation. When the depletion regions merge, majority carriers in the source enter into the substrate and get collected by the drain, and punch through takes place.

III. SURVEY OF LEAKAGE REDUCTION TECHNIQUES

A.MTCMOS-(Multi-threshold CMOS)

A high-threshold NMOS gating transistor is connected between the pull-down network and the ground, and low-threshold voltage transistors are used in the gate. The reverse conduction paths exist, which tends the noise margin to reduce or may result in complete failure of the gate. There also exists a performance penalty due to the high-threshold transistors in series with all the switching current paths. Dual VT technique is a variation in MTCMOS, in which the gates in the critical path use low-threshold transistors and high-threshold transistors for gates in non-critical path [1], [2]. Both the methods requires additional mask layers for each value of V_{th} in fabrication, which is a complicated task depositing two different oxides thickness, hence making the fabrication process complex.

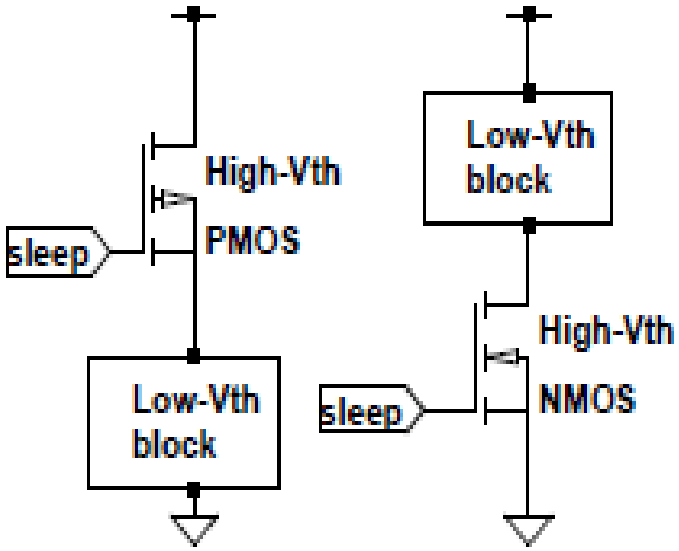

Fig3.1. MTCMOS technique

The techniques also suffer from turning-on latency i.e., the idle subsections of circuit cannot be used immediately after reactivated since some time is needed to return to normal operating condition. The latency is typically a few cycles for former method, and for Dual technology, is much higher. When the circuit is active, these techniques are not effective in controlling the leakage power.

B. SLEEP Transistor Technique

This is a State-destructive technique which cuts off either pull-up or pull-down or both the networks from supply voltage or ground or both using sleep transistors. This technique is MTCMOS, which a high-Vth sleep transistors between pull-up networks and V_{dd} and pull-down networks and gnd while for fast switching speeds, low-Vth transistors are used in logic circuits [3]. Isolating the logic networks, this technique dramatically reduces leakage power during sleep mode. However, the area and delay are increased due to additional sleep transistors. During the sleep mode, the state will be lost as the pull-up and pull-down networks will have floating value. These values impact the wakeup time and energy significantly due to the requirement to recharge transistors which lost state during sleep.

C. Forced Stack

In this technique, every transistor in the network is duplicated with both the transistors bearing half the original transistor width [4]. Duplicated transistors cause a slight reverse bias between the gate and source when both transistors are turned off. Because sub-threshold current is exponentially dependent on gate bias, it obtains substantial current reduction. It overcomes the limitation with sleep technique by retaining state but it takes more wakeup time.

D. ZIGZAG Technique

Wake-up cost can be reduced in zigzag technique but still state losing is a limitation. Thus, any particular state which is needed upon wakeup must be regenerated somehow. For this, the technique may need extra circuitry to generate a specific input vector.

E. SLEEPY STACK Technique

This technique combines the structure of the forced stack technique and the sleep transistor technique. In the sleepy stack technique, one sleep transistor and two half sized transistors replaces each existing transistor [5]. Although using of W0/2 for the width of the sleep transistor, changing the sleep transistor width may provide additional tradeoffs between delay, power and area. It also requires additional control and monitory circuit, for the sleep transistors.

F. LEAKAGE FEEDBACK Technique

This technique is based on the sleep approach. To maintain logic during sleep mode, the leakage feedback technique uses two additional transistors and the two transistors are driven by the output of an inverter which is driven by output of the circuit implemented utilizing leakage feedback. Performance degradation and increase in area are the limitations along with the limitation of sleep technique.

G. SLEEPY KEEPER Technique

This technique consists of sleep transistors connected to the circuit with NMOS connected to Vdd and PMOS to Gnd. This creates virtual power and ground rails in the circuit, which affects the switching speed when the circuit is active [6]. The identification of the idle regions of the circuit and the generation of the sleep signal need additional hardware capable of predicting the circuit states accurately, increasing the area requirement of the circuit. This additional circuit consumes power throughout the circuit operation to continuously monitor the circuit state and control the sleep transistors even though the circuit is in an idle state.

H. Super Cutoff CMOS Technique (SCCMOS)

This technique has been proposed to solve the problem of the extra cost of the MT approach [7]. The basic idea behind this method is to turn off completely the transistor which connects the maincircuit to VDD or GND. This is achieved by connecting the gate of the transistor to a voltagewhich is higher than VDD. This leads to a positive Vgs for a PMOS transistor and, hence the sub threshold current reduces exponentially with increasing this voltage.

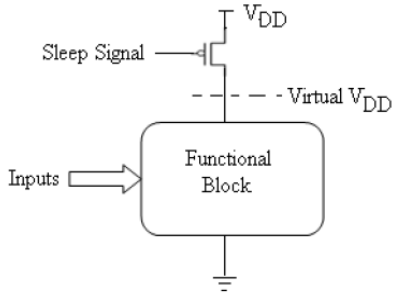

Fig.3.8 Super Cutoff CMOS Technique (SCCMOS)

E. VCLEARIT Technique

The block diagram for VCLEARIT technique is presented in Fig.3.9. VCLEARIT [9] CMOS technique, the normal operating mode, 'sleep' is 'off' and 'sleepbar' is 'on'. This causes transistors {P0, N0} to turn off and transistor P1 to turn on. The circuit now behaves exactly as a normal CMOS complementary circuit. The sleep (standby) operating mode is a little more involved. In this mode, 'sleep' is on and 'sleepbar' is off. Hence transistors {P0, N0} turn on and transistor P1 turns off. Since P0 is on, common point X1 is also at voltage Vdd. The pull-up (PUN) is now between two points at equal voltage potential (Vdd) and hence no leakage current should flow through the PUN.

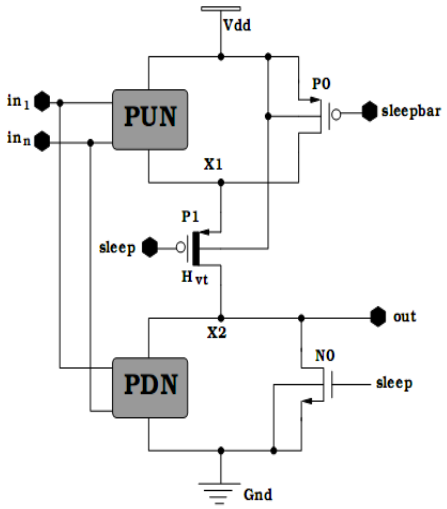

Fig.3.9. Generic VCLEARIT CMOS Technique

Similarly, N0 is on and common point X2 is grounded. The pull-down (PDN) is now between two points at equal voltage potential (Gnd) and hence no leakage current should flow through the PDN. Since 'out' is connected to X2, during the sleep mode the output value will always be '0'. The leakage loss occurring during the sleep mode will only be through the high - Vth transistor P1 which is turned off, but, connected between points X1 and X2 that are at different voltage potentials.

F. LECTOR Technique

Leakage Control Transistor technique (LECTOR) introduces LCTin each CMOS gate as shown in Fig.3.9. Since one of the LCTs is always near its cut off, it causes increase in resistance in the path from VDD to ground leading to decrease in leakage current [10]. LECTOR is single threshold, vector independent method which requires only two transistors for every path in a circuit.

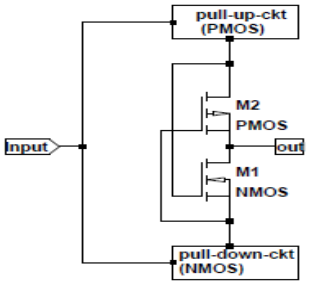

Fig.3.9. LECTOR Technique

In this arrangement, one of the LCTs is always "near its cutoff voltage" for any input combination. This increases the resistance of the path from Vdd to ground, thereby decrease in leakage currents. The significant feature of LECTOR is that it works effectively in both active and idle states of the circuit, resulting in better leakage reduction. The basic idea behind the approach for reduction of leakage power is the effective stacking effect of transistors in the path from supply voltage to ground.

IV. PROPOSED METHOD

A. GALEOR Method

In this technique the maximum reduction in leakage power is achieved by introducing high threshold voltage transistors, thereby increasing circuit delay. It reduces theleakage current flowing through the circuit. In this technique two gated leakage transistors are inserted between NMOS and PMOS circuitry of the existing circuit such that gates of the extra inserted transistors are connected to their respective drain regions. The block diagram of GALEOR technique is shown in Fig.4.1.

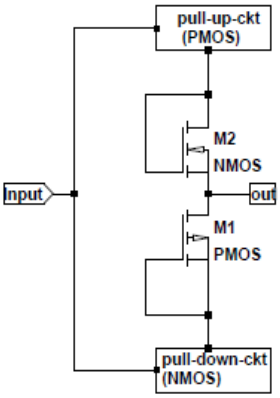

Fig.4.1. GALEOR Technique

B.Benefit of GALEOR Technique

GALEOR provides two Leakage Control Transistors (LCTs), a p-type and an n-type within the logic gate for which the gate terminal of each LCT is controlled by the source terminal of the other. The LCTs are self-controlled and do not require any control logic unlike in the popularly used sleep transistor method. GALEOR is effective in both idle and active states of the circuit resulting in better leakage reduction. GALEOR reduces leakage power without increasing switching power. It does not require additional circuitry for monitoring thestates of the overall circuit. This cuts the dynamic power dissipationof the additional circuitry which has to be active even when overall circuit is idle. Either one of the two LCTs is always "near its cut-off voltage" for any input vector combination, thus increasing the stacking effect without any additional control signals.

V. CONCLUSION

In this paper, we proposed a GALEOR technique effectively enhances the reduction of subthreshold and gate oxide leakage simultaneously.When increase in leakage power because of the scaling down of device dimensions, supply and threshold voltages in order to achieve high performance and low dynamic power dissipation, becomes more with the deep-submicron and nanometer technologies and thus it becomes a great challenge to tackle the problem of leakage power. GALEOR achieves the reduction in leakage power compared to other leakage reduction techniques, such as LECTOR, sleepy stack, sleepykeeper, etc.., along with the advantage of not affecting the dynamic power, since this technique does not require any additional control and monitor circuitry and also in this technique, the exact logic state is maintained.

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