RESEARCH ARTICLE

A NOVEL DESIGN OF CURRENT MODE MULTIPLIER/DIVIDER CIRCUITS FOR ANALOG SIGNAL PROCESSING

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Abstract- In analog signal processing, current is used as input variables. In this design current mode multiplier /divider circuits is implemented in two modes. Thus implementing the circuit with proposed concept has very small linearity errors. In addition, high linearity is achieved because high accuracy current mirrors are adopted and the output current is insensitive to the temperature. The proposed computational structures are designed for implementing in 0.18-µm CMOS technology, with a low-voltage operation (a supply voltage of 1.2 V) excepting with the power consumptions are 55 and 70 µW, respectively, while their frequency bandwidths are 79.6 and 59.7 MHz, respectively.

Index Terms- Analog signal processing, current-mode operation, multiplier

I. INTRODUCTION

Signal processing circuits find a multitude of applications in many domains such as telecommunications, medical equipment, hearing devices, and disk drives [1]–[4], the preference for an analog approach of signal processing systems being mainly motivated by their low-power operation and high speed that allows a real-time signal processing.

Analog signal processing represents the signals as physical quantities like e.g. charge, current, voltage or frequency. These signals are continuous in value and continuous in time. Analog signal processing is most effective when precision is not the major criteria and when massive parallel collective processing of large number of signals that are continuous in time and amplitude is required [2]. Multiplication and division of analog signals are difficult operations in analog signal processing.

Analog multipliers and dividers are used in communication circuits as well as in neural networks and fuzzy logic applications. Phase detector, adaptive filter, function generators, frequency doubling and amplitude modulation are some applications of analog multipliers in communications industry. Voltage gain amplifier, signal squarer, RMS signal estimator and weight-input multiplication in neural networks are some application in signal processing .Analog multipliers as part of automatic gain control circuits used in AM radio receivers and radar system. Low supply voltages, low bias currents, low effective threshold voltages of MOS transistors are some methods to reduce power consumption in multiplier and divider architectures.

In order to improve the frequency response of the computational structures and to increase their −3 dB bandwidth, many analog signal processing functions can be achieved by exploiting the squaring characteristic of MOS transistors biased in saturation. In [3], multiplier structures were presented with single-ended input voltages, the linearization of their characteristics being obtained using proper squaring relations between the input potentials. In order to implement the multiplication of two differential-input voltages, in [5] multiplier circuits were described based on mathematical principles, similar to the methods used for multipliers with single input voltages. The biasing of the multiplier differential core at a current equal to the sum of a constant component and a current proportional to the square of the differential input voltage was presented in [7] and [8] and allows us to obtain a linear behavior of the implemented multiplier circuits. In another class of multipliers [7]–[9], currents are used as input variables. In this case, the designed circuits present the advantage of an independence of the circuit performances on technological errors. These circuits can implement, based on the same configuration, both multiplying, and dividing functions. Multiplier structures were also reported [24]–[28] with increased linearity, designed using different mathematical principles.

II.   THEORETICAL ANALYSIS

The main goal of the proposed designs is related to the accuracy of implemented functions. The current-mode approach of the multiplier/divider circuits strongly increases their frequency response. A further advantage of the independence of the computational circuit's output currents on technological parameters is that it contributes to an important increase in the accuracy of the multipliers and dividers. Additionally the operation of the proposed circuits is not affected by the temperature variations.

A. First Multiplier/Divider Circuit

The first original proposed implementation of a current mode multiplier/divider circuit is presented in Fig. 1.The equations of the functional loops containing M1, M2, M3, and M4 gate-

source voltages can be expressed as follows:

$$2V_{GS}(I_2) = V_{GS}(_{ID1,2}) + V_{GS}[I_{D1,2} + 2(I_1 + I_0)] \qquad (1)$$

Thus, considering the squaring characteristics of MOS transistors biased in the saturation region

$$I_{D1,2} = I_2 - (I_1 + I_0) + \frac{(I_1 + I_0)^2}{4I_2} \qquad (2)$$

The expression of the output current will be $I_{OUT} = I_{D2} - I_{D1} + 2I_O$, resulting in $I_{OUT} = I_O I_1/I_2$. So, the circuit implements the multiplying/dividing function, having the advantage of an independence of the output current expression on technological parameters and of a circuit operation that is not affected by temperature variations.
The aspect ratios of MOS transistors from Fig. 1 are as follows: M1–M8 4.5/0.9; M9, M14, M16, M17 5.4/0.9; M10–M13, M15 10.8/0.9. The chip area of the multiplier/divider implemented in 0.18-µm CMOS technology, shown in Fig. 1, equals approximately 600 µm2 (including pads).

B. Second Multiplier/Divider Circuit

The second original realization of the multiplier/divider circuit is presented in   Fig. 2. The equation of the functional loop containing M1, M2, M4, and M5 gate-source voltages can be expressed as follows:

$$2V_{GS}(I_2) = V_{GS}(I_{OUT1}) + V_{GS}[I_{OUT1} + 2(I_1 + I_O)] \qquad (3)$$

Thus,

$$I_{OUT1} = I_2 - \frac{2(I1 + I0)}{2} + \frac{4(I1 + I0)2}{16I2} \qquad (4)$$

A similar expression can be obtained for the I_{OUT2} current, replacing in (4) the $(I_1 + I_O)$ current with $(I_1 - I_O)$ current. The expression of the output current of the multiplier/divider circuit from Fig. 2 is $I_{OUT} = I_{OUT1} - I_{OUT2} + 2I_O$, resulting $I_{OUT} = (I_O I_1)/I_2$. The aspect ratios of MOS transistors from Fig. 2 are as follows: M1–M5, M7–M11, M13–M15, M18–M23 4.5/0.9; M6, M12 10.8/0.9; M16, M17 9/0.9. The chip area of the multiplier/divider implemented in 0.18-*μ*m CMOS technology, shown in Fig. 2, equals approximately 800 *μ*m2 (including pads). The negative feedback loops that enforce M4 and M15 transistors and, respectively, M8 and M18 transistors to have the same current are stable, since their speed is suitable for obtaining the requested frequency response for the designed circuits.

III.   ERRORS INTRODUCED BY SECOND-ORDER EFFECTS

The most important errors introduced in the multiplier/divider circuit's operation are represented by the mismatches, channel effect modulation, body effect, and mobility degradation. As a result of these undesired effects, the proper functionality of previous circuits will be affected by additive errors. The values of these errors are relatively small because second-order effects are smaller with a few orders of magnitude than the main squaring characteristic that models the MOS transistor operation. Additionally, a multitude of specific design techniques exist that are able to compensate the errors introduced by the second-order effects. The practical realization of translinear loops using common-centroid MOS transistors strongly reduces the errors introduced by the mismatches between the corresponding devices. The design of current mirrors using cascade. This configuration allows an important reduction of the errors caused by the channel length modulation. In this situation, a tradeoff between the impact of the second-order effects and the minimal value of the supply voltage must be performed. Because the bulks of an important number of MOS transistors from Figs. 1 can be connected to their source, the errors introduced by the bulk effect can be canceled out for these devices.

Small-Signal Frequency Response of Multiplier/Dividers

The multiplier/divider circuit proposed in Fig. 1 is designed for allowing a high bandwidth. In order to achieve this goal, there exists a single high-impedance node, noted with A, which will impose the maximal frequency of response of the circuit from Fig. 1, because in Fig. 2 there exist three high-impedance nodes (A, B, and C). As most of the nodes in a circuit represent low-impedance nodes, it is expected that the proposed circuits to have relatively high maximal frequencies of operation (79.6MHz respectively, obtained after simulations).

IV.   SIMULATED RESULTS

The I_{OUT} (I_1) simulation for the first multiplier/divider circuit proposed in Fig. 1, for an extended range of I_1 current (between 0 and 10 μA), is presented in Fig. 3. The I_O current is set to be equal to 40 μA, while the I_2 current has a parametric variation: 1) 10 μA; 2) 20 μA; 3) 30 μA; and 4) 40 μA. The I_O current is a sinusoidal current with a frequency of 1 MHz and an amplitude equal to 200 μA, the I_1 current is a sinusoidal current having a frequency of 60 MHz and an amplitude equal to 300 μA, while I_2 is a constant current equal to 300 μA. The simulations were made using the BSIM4 model, associated with a 0.18-μm CMOS process, MOS active devices having fT = 3.5 GHz. Comparing with alternative implementations in 0.35 μm CMOS technology of the proposed multiplier/divider structures, some important advantages can be achieved. The supply voltage can be decreased from 3 to 1.2 V, correlated with a relatively important decrease of the circuits' power consumption. Additionally, the circuits' bandwidths can be increased by their implementation in 0.18-μm CMOS technology.
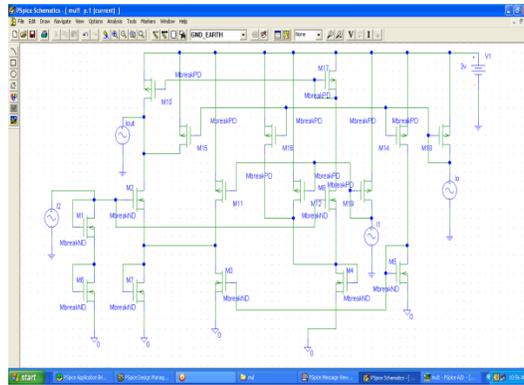
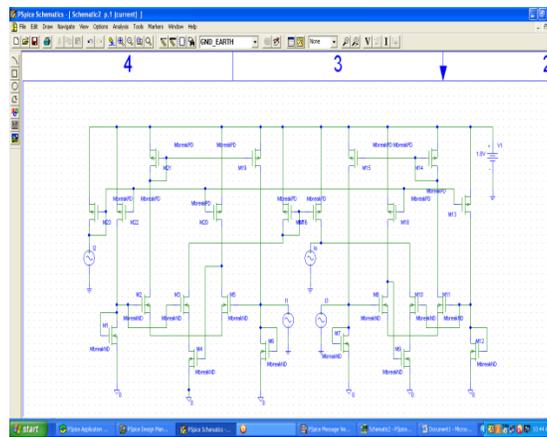Fig.1.First current Mode Multiplier/Divider
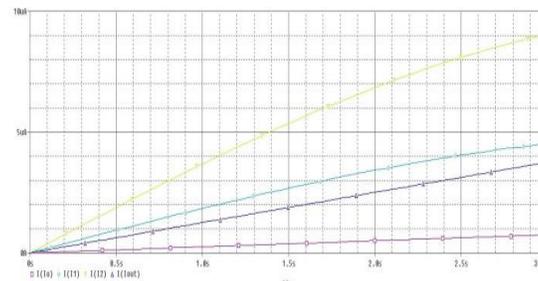

Fig.2.Second multiplier/divider circuit

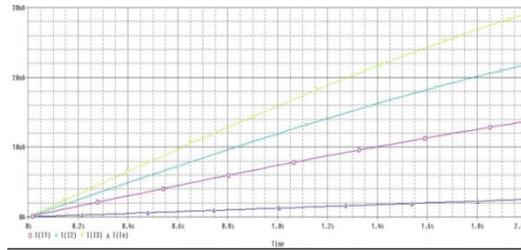Fig.3. I_{OUT} (I_1) simulation for the first multiplier/divider circuit

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Fig.4. I_{OUT} (I_1) simulation for second multiplier/divider circuit
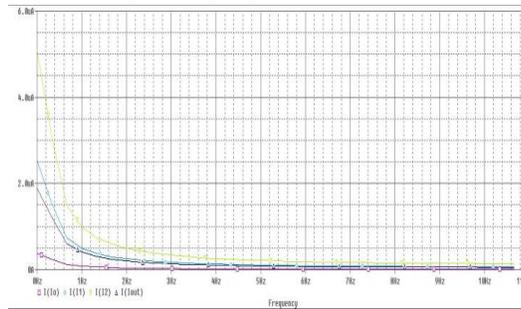

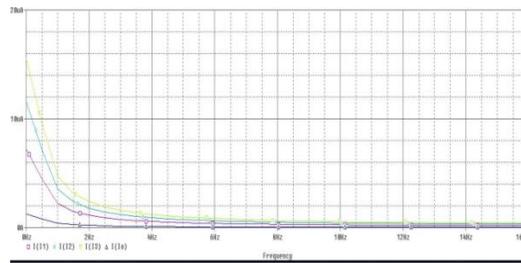Fig. 5. I_{OUT} (I_2) simulation for the first multiplier/divider circuit.

Fig. 6. I_{OUT} (I_2) simulation for the second multiplier/divider circuit

TABLE I
COMPARISON BETWEEN THE PROPOSED MULTIPLIER/DIVIDER CIRCUITS AND PREVIOUS
REPORTED WORK

Parameters	Ref. no 1	Proposed work	
		Fig.1(this brief)	Fig.2(this brief)
Technology[μm]	0.35	0.18	0.18
Supply Voltage [V]	3.3	1.2	1.2
Power Consumption[μW]	210	55	70
Chip Area [μm^2]		600	800
Bandwidth [MHz]	41.4	79.6	59.7

The proposed multiplier/divider structures have the most important advantages, such as the smallest linearity error and an increased bandwidth, compared with previously reported circuits. The circuits were designed for implementing in 0.18- μm CMOS technology, being supplied at 1.2 V. The proposed structures have extremely low linearity errors (0.75% and 0.9%, respectively). The minimal value for the supply voltage of 1.2 V was obtained for implementing the proposed computational structures in 0.18-μm. If the range of input currents is limited to 0–5 μA, the power consumptions of both proposed multiplier/divider circuits (60 and 75 μW, respectively) are smaller than the power consumption of most previously reported circuits. The input referred noise is smaller than 0.6 6V/√Hz for both proposed multiplier/divider structures.

V.   CONCLUSION

This brief presented two original improved accuracy multiplier/divider circuits. The current-mode operation of the proposed computational structures further increases the circuit's accuracy; while the removal of the impact of temperature variations on the circuits' operation additionally contributes to increase the performance of the multiplier/dividers .The proposed structures have extremely low linearity errors (0.75% and 0.9%, respectively). The minimal value for the supply voltage of 1.2 V was obtained for implementing the proposed computational structures in 0.18- μm. The circuits bandwidth are 79.6 and 59.7 MHz, respectively, while their power consumptions are extremely, low (55 and 70 μW, respectively).Another important factor that contributes to the small value of the minimal supply voltage is represented by the proposed architectures of the multiplier/divider circuits, compatible with low-voltage operation (avoiding any cascade stages and having a current-mode operation).

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