Available Online at www.ijcsmc.com

International Journal of Computer Science and Mobile Computing

A Monthly Journal of Computer Science and Information Technology

ISSN 2320–088X

IJCSMC, Vol. 4, Issue. 10, October 2015, pg.420 – 427

RESEARCH ARTICLE

A New Topology of Single-Phase Nine-Level Inverter with Less Number of Power Elements for Grid Connection

C Surekha[1], Jeetender Vemula[2]

[1]M.Tech Student (PE&ED), Vignana Bharathi Institute of Technology, Hyderabad
Email: chenisurekha@gmail.com

[2]Assistant Professor, EEE Dept., Vignana Bharathi Institute of Technology, Hyderabad
Email: jitender.vemula1987@gmail.com

Abstract- Recently, the evolution of single phase multilevel inverters has been escalation due to its preference over traditional one. In this paper proposed a new topology of single phase Nine level inverter with less number of power elements for grid connection. In this proposed inverter have ten switches and their switches operate with fundamental frequency. The proposed inverter produced nine level output voltage from three input voltage sources. The proposed inverter reduced the switching losses (because of all switches operate with fundamental frequency), complexity, control circuit and place requirement. The proposed inverter compared to a single-phase seven level pulse width modulation (PWM) inverter for grid connection. The proposed inverter compared to conventional inverter has PWM technique have two triangular carrier signals identical to each other with an offset equivalent to the amplitude of the reference signal were used to generate PWM signals for the switches. The proposed inverter compared to conventional inverter has some switches operate at fundamental frequency and other operates at switching frequency.

I. INTRODUCTION

Multilevel inverters (MLI) started with the neutral point clamped inverter topology proposed by Nabae et al. [1]. Presently multilevel inverters have become more attractive for researchers due to their advantages over conventional three-level Pulse width-modulated (PWM) inverters. MLI has two main advantages compared with the conventional H-bridge inverters [2]-[4], the higher voltage capability and the reduced harmonic content in the output waveform due to the multiple dc levels. MLI is now preferred in high power medium voltage applications due to the reduced voltage stresses on the devices. MLI incorporates a topological structure that allows a desired output voltage to be synthesized among a set of isolated or interconnected distinct the voltage sources.

Numerous topologies realize this connectivity and can be generally divided into three major categories namely, diode clamped MLI, flying capacitor MLI and separated dc sources (cascaded voltages) MLI [5].

Recently nonconventional energy sources for grid connected applications are increased due to the world energy crisis. Injecting power to the utility must meet the world harmonic standards. Therefore, single phase MLIs become a good solution for most particular demerits of MLI is the large number of the required power semiconductor switches. Although low voltage rate switches can be utilized in a multilevel inverter, each switch requires a related gate drive circuit. This may be problem occurs, the overall system to be more expensive and complex. So, in practical implementation, decreasing the number of switches and gate driver circuits have become an essential point.

Recently, so many topologies of the MLI and its control techniques have been published. The MLI technique is implemented in [8] by adding one switch and four power diodes to the H-bridge single phase inverter. Another solution can be found in [9] by using two switches and two power diodes with the H-bridge single phase inverter. Those two systems can generate only five levels in the output voltage with less harmonic contents. The other solution, shown in [10], is a modular inverter that can each to any required voltage levels. But these inverters topologies can be improved by reducing their switches without affecting their performances.

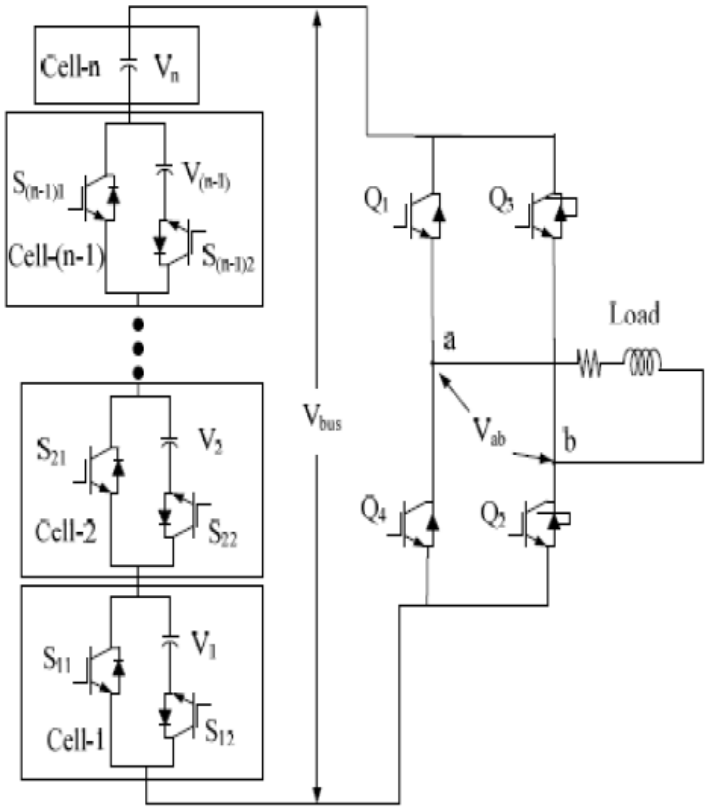
This paper presents a conventional inverter single-phase five-level PWM inverter with less number of power elements and hence less gate drive circuits in addition to less circuit layout complexity. Its output voltage has the following five levels: zero, +Vdc, +0.5Vdc, -0.5Vdc and -Vdc. As the number of output levels increases the harmonic content can be reduced. This inverter topology uses two carrier signals to generate PWM signals for the switches. Some switches operate at fundamental frequency and others operate at switching frequency. Sections II and III explain the principle of operation and PWM strategy for the proposed inverter respectively. The switching algorithm that used in PWM is presented in section IV.

In this paper proposed a new topology of single phase seven level inverter with less number of power elements for grid connection.

The proposed inverter produced seven level output voltage from two input voltage sources. The seven level output voltages produces are zero, +1.5Vdc, +Vdc, +0.5Vdc, -0.5Vdc, -Vdc and -1.5Vdc. In this proposed inverter have eight switches and their switches operate with fundamental frequency compared to the seven level produced by 12 switches in cascaded H-bridge configuration. The proposed inverter reduced the switching losses (because of all switches operate with fundamental frequency), complexity, control circuit and place requirement. The THD analysis is as shown in MATLAB/Simulink.

II. OPERATIONAL PRINCIPLES OF THE CONVENTIONAL INVERTER

Figure 1 shows the conventional structure single phase MLI inverter. It consists of 'n' cells of switch circuits. For cells from '1' to (n-1), each k-cell is composed of one dc voltage source and two switches (Sk1,Sk2); one switch (Sk2) is connected in series with a dc voltage source and the other switch (Sk1) is connected in parallel with both the dc voltage source and the series switch. Based on this configuration, each cell can generate two states (0V) and the dc voltage source associated with the considered cell. Cell 'n' is composed of only the dc source voltage resulting in generating only one state (Vn). As a result, the dc link voltage Vbus has (n-1) states, they are (V1, V2…., Vn), as shown in Fig.2.



Figrue.1 Structure of the conventional cascaded dc link MLI The above figure shows Structure of the conventional cascaded dc link MLI

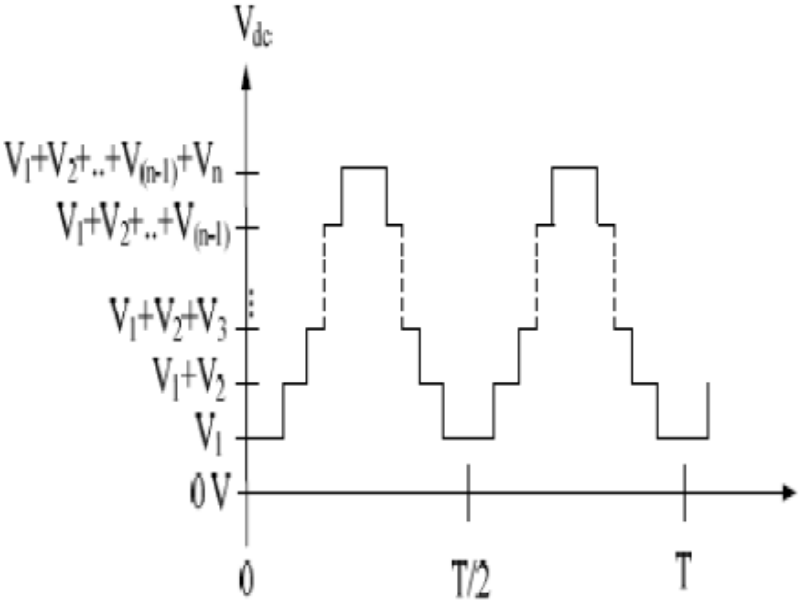


Figure.2 Typical output waveform of Vdc

The above figure shows typical output waveforms of Vdc It can be noted that the dc link voltage has no zero state voltage (0v) which needs extra two main switches. The H-bridge inverter composes of four switches (Q1, Q2, Q3 and Q4). The H-bridge inverter has two functions; it has to synthesis the inversion voltage of the dc link voltage in addition to generating the zero state voltage (0v) at the output voltage (Vab) by connecting the upper two switches (Q1, Q3) or the lower switches (Q2, Q4). Obviously, this structure can reduce the number of switches compared to the conventional topologies without affecting the inverter performances. This is due to that; the zero voltage can be generated using the idea of the upper or lower H-bridge inverter to generate this state. The pulse width modulation (PWM) control algorithm can be applied also for this topology. The PWM control algorithm, which adopted in this paper, consists of one modulation signal with amplitude (Ar) an n (number of dc link cell) carriers with same amplitude (Ac) from the former one. The amplitude (Ar) can be changed from 0 to n*Ac according to changing modulation index from 0 to 1.

III. SINGLE-PHASE SEVEN –LEVEL PWM INVERTER

Figure 3 shows that multilevel inverter is a new topology of a single-phase seven level inverter with less number of power elements for grid connection. The seven level output voltage produced by the above inverter. This topology of an inverter has eight switches and two sources and grid connection. This inverter output voltage is connected to the grid. In the cascaded H-bridge configuration, seven level output voltage produced by using 12 switches. But in this new topology, seven level output voltage produced by using 8 switches. The seven level output voltage switching strategy as shown in the below table I.

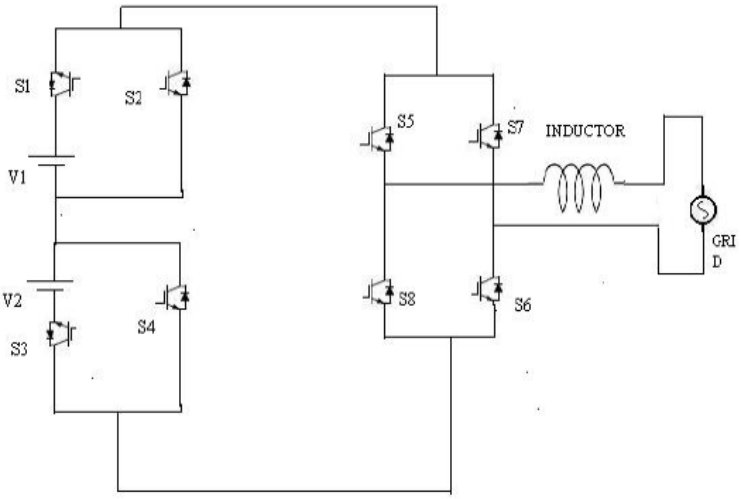


Figure.3 Conventional single-phase seven-level inverter with less number of power elements for grid connection

TABLE I THE 7 LEVEL OUTPUT VOLTAGE SWITCHING STATES

Output voltage levels	Switching states							
	S_1	S_2	S_3	S_4	S_5	S_6	S_7	S_8
+1.5Vdc	ON	OFF	ON	OFF	ON	ON	OFF	OFF
+Vdc	OFF	ON	ON	OFF	ON	ON	OFF	OFF
+0.5Vdc	ON	OFF	OFF	ON	ON	ON	OFF	OFF
0	OFF	OFF	OFF	OFF	ON	OFF	ON	OFF
-0.5Vdc	ON	OFF	OFF	ON	OFF	OFF	ON	ON
-Vdc	OFF	ON	ON	OFF	OFF	OFF	ON	ON
-1.5Vdc	ON	OFF	ON	OFF	OFF	OFF	ON	ON

The switching sequence of seven level output voltage produced in the proposed inverter explain below.

1. The +1.5Vdc output voltage produced by using the switches are S3, S5 and S6 are ON position in the proposed inverter.

2. The +Vdc output voltage produced by using the switches are S3, S2 and S5 are ON position in the proposed inverter.

3. The +0.5Vdc output voltage produced by using the switches are S1,S4, S5 and S6 are ON position in the proposed inverter.

4. The 0 Volts voltage produced by using switches are S5, S7 are ON position in the proposed inverter.

5. The -0.5Vdc output voltage produced by using the switches are S1,S4, S7 and S8 are ON position in the proposed inverter.

6. The -Vdc output voltage produced by using the switches are S2, S3, S7 and S8 are ON position in the proposed inverter.

7. The -1.5Vdc output voltage produced by using the switches are S1, S3, S7 and S8 are ON position in the proposed inverter.

The advantages of proposed inverter is
1. The seven level output voltage produced by using 8 switches.
2. All switches are operated with fundamental frequency.
3. Switching losses are reduces.
4. Circuit complexity reduces.
5. Control circuit reduces.
6. Number of cooling equipment, protection circuit reduces.
The seven level output voltage as shown below figure.

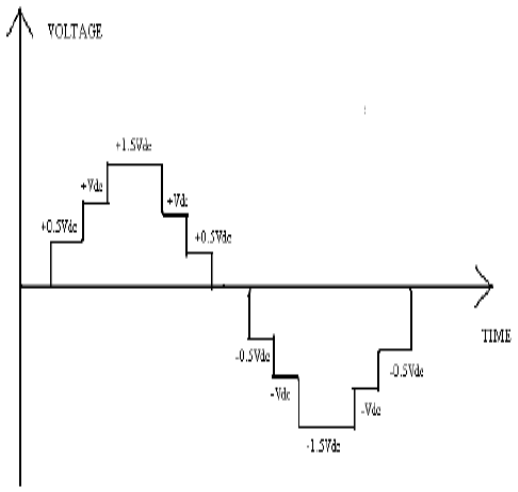


Figure.4 the seven level output voltage produced by the conventional inverter

IV. PROPOSED NINE-LEVEL INVERTER

To demonstrate the operation of the proposed inverter, a nine-level configuration, which is shown in Fig.5, is used. As it is shown in Fig. 4, the structure consists of four transformers, eight unidirectional switches and a bidirectional switch. There are also four modules in this structure. Each module can generate two voltage levels positive (+Vdc) and negative (-Vdc) except the last module with three switches which can create three voltage levels positive (+Vdc), zero, negative (-Vdc).

Therefore, the zero voltage level can only be generated by the last module with three switching devices. The maximum output voltage level can be generated from this structure is +4Vdc. Table 1 shows the switching pattern of the inverter shown in Fig. 4 for different output voltage levels. It is worth noting that various switching states are possible for the same voltage level. For instance, to generate the output voltage of the +Vdc, switches S1, S3, S6 and S bidirectional are turned on. It is also possible to obtain the same output voltage by turning on the switches S1, S4, S5 and S bidirectional.

There are several modulation strategies for multilevel inverters and operation of them depends on modulation strategies [13 – 15]. The modulation methods used in multilevel inverters can be categorized according to switching frequency. In this paper, the fundamental frequency switching technique has been employed. It is important to note that the calculation of optimal switching angles for different purposes such as elimination of the selected harmonics and minimizing THD are not the objective of this paper.

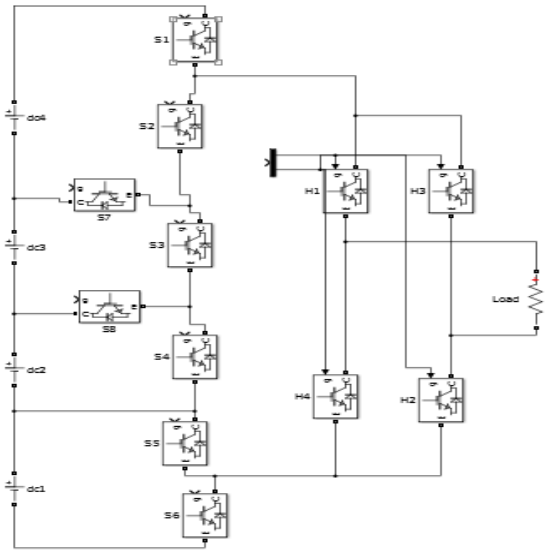


Figure.5 Proposed Nine-Level Inverter

Output Voltage Level	S1	S2	S3	S4	S5	S6	S7	S8	S bidirectional
+4Vdc	On	Off	On	Off	On	Off	On	Off	Off
+3Vdc	On	Off	On	Off	On	Off	Off	Off	On
+2Vdc	On	Off	On	Off	On	Off	Off	On	Off
+Vdc	On	Off	On	Off	Off	On	Off	Off	On
0	On	Off	On	Off	Off	On	Off	On	Off
-Vdc	Off	On	Off	On	On	Off	Off	Off	On
-2Vdc	Off	On	Off	On	Off	On	On	Off	Off
-3Vdc	Off	On	Off	On	Off	On	Off	Off	On
-4Vdc	Off	On	Off	On	Off	On	Off	On	Off

Table II. Output voltage for various states of switches

A. Comparison Study

The present paper aims to reduce the number of components used in multilevel inverter. There is only a single DC source used in this structure. The number of switching devices required to realize an m-level output voltage in conventional cascaded H bridge inverters is as follows:

SW = 2m – 2 (4)

The numbers of switches in the proposed structure are compared with the cascaded H-bridge multilevel inverter in Fig. 5. As it is shown in Fig. 5, the proposed structure requires fewer switching components. Each switching device requires a gate driver to operate. Therefore, reduction in the number of switching devices also results in fewer number of gate drivers which leads to a smaller size and lower cost of the implementation.

The number of on switches is also an important criterion to compare the structures. There are two on switches in each module of the conventional H-bridge inverter. However, the number of on switches in each module of the proposed inverter is one. More number of on switches means more voltage drop on these switches. The number of on switches for an m-level output voltage in conventional cascaded H-bridge inverter can be calculated as follows:

Non = m-1 (5)

The number of on switches in the proposed structure can be given as follows:
Non = (m-1)/2 (6)
Where m is the number of output voltage levels.

V. SIMULATIONS AND RESULTS

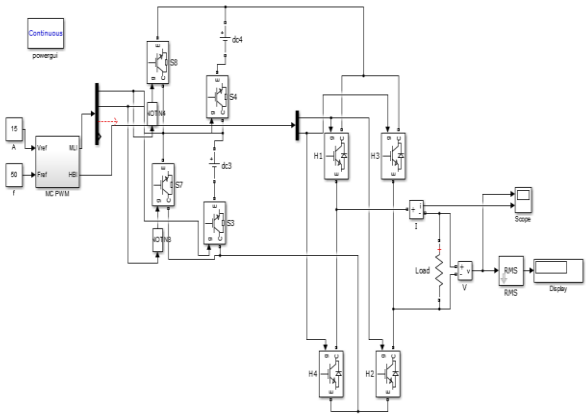


Figure.6 Simulation of Conventional Seven-Level Inverter

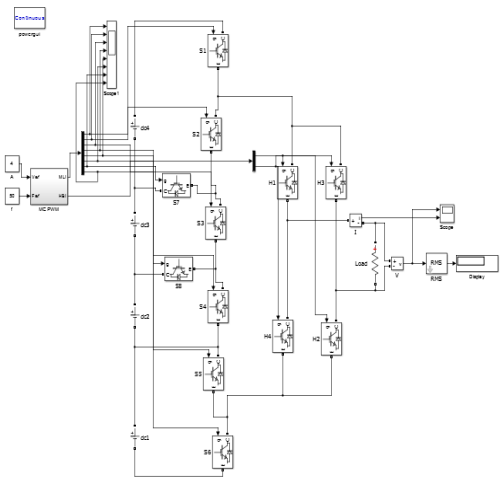


Figure.7 Simulation of Proposed Nine-Level Inverter

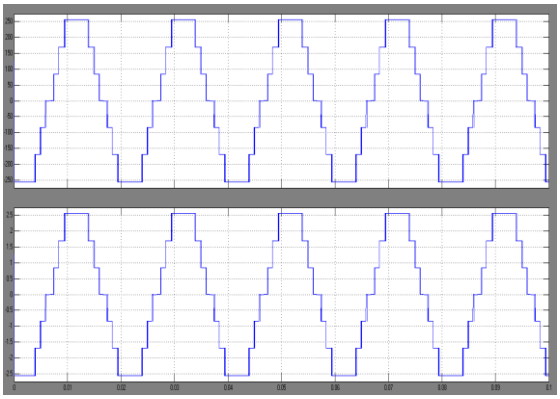


Figure.8 Seven Level Output Voltages and Currents

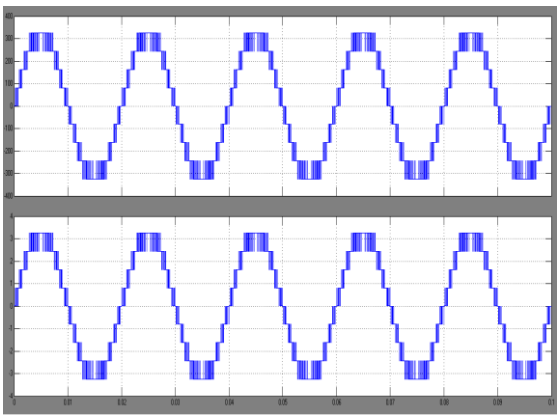


Figure.9 Nine Level Output Voltages and Currents

VI. CONCLUSION

In this paper, a novel topology for cascaded multilevel inverters is presented. The proposed structure benefits from the advantage of fewer numbers of components. The number of switching devices as well as the number of gate drivers is reduced in the proposed topology. Therefore, the size and the cost of implementation are decreased. To validate the proper operation of the proposed structure, simulation and experimental results are provided. For the modified configuration a comparison between seven level and nine level inverters has been done.

REFERENCES

[1] Nabae.A., Takahashi.I., and Akagi. H., "A new neutral-point clamped PWM inverter", IEEE transactions on Industrial Applications, Vol. IA-17, pp. 518-523, September/October 1981.

[2] Siriroj Sirisukprasert, Jih-Sheng Lai and Tian-Hua Liu, "Optimum harmonic reduction with a sied range of modulation indexes for multilevel converters", IEEE Transactions on Industrial on Electronics, Vol.49,Issue 4, pp.875-881,August-2002.

[3] Brendan Peter McGrath and Donald Grahame Holmes, "Multicarrier PWM strategies for multilevel inverters", IEEE Transactions on Industrial Electronics, Vol.49, Issue4, pp.858-867, August 2002.

[4] Lai.J.S., and Peng, F.Z., "Multilevel converter- a new breed of power converters, "IEEE Transactions on Industrial Applications, vol.32, Issue3. Pp.509-517, May/Jun 1996.

[5] Villanueva. F, Correa, P, Rodriguez. J, Paca. M, "Single-phase Cascaded H-bridge Multilevel inverter for Grid connected photovoltaic systems:, IEEE Transactions on Industrial Electronics, Vol.56, Issue 11,2009,pp 4399-4406.

[6] P. Panagis, P. Stergiopolos, S. Manios, "Comparison of state of the ar t multi level inverters ", Proc. Power Electronics Specialists Conf., Rhodes, PESC, 2008, pp. 4296-4301.

[7] F.Z. Peng, J.S. Lai, "Multilevel converters—A new breed of power converters", IEEE Trans. Ind. Application., vol. 49, no. 3, pp. 509 - 517, May/June, 1996.

[8] E. Zeliang, D. Na, C. Jie and Z. Haifeng, "A Simple Voltage Balancing Scheme for m-Level Diode-Clamped Multilevel Converters Based on a Generalized Current Flow Model", IEEE Trans on Industrial Electronics, vol. 60, no. 5, pp. 1884 - 1896, April, 2013.

[9] H. Sepahvand, K.A. Corzine, M. Ferdowsi, M. Khazraei, "Active Capacitor Voltage Balancing in Single-Phase Flying-Capacitor Multilevel Power Converters", IEEE Trans on Industrial Electronics, vol. 59, no. 2, pp. 769 - 778, April, 2012.

[10] Y. Suresh and A.K. Panda, "Performance of cascade multilevel H-Bridge inverter with single DC source by employing low frequency three-phase transformers", 6th Annual Conference on IEEE Industrial Electronics Society, Glendale, AZ,. IECON. 2010, pp. 1981 - 1986.

