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A POPBL CONCEPTUAL FRAMEWORK FOR THE DESIGN AND IMPLEMENTATION OF ASICs

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Abstract— The popularity of ASICs is growing every day due to the high demand for customization and the need for hardware/software integration in the digital society, especially in the IoT. A major benefit of using custom ASIC models in IoT is that products delivery can be carried out at very low cost thus, making the designers across the vertical market like industrial, smart utilities and medical devices to differentiate IoT products using custom ASIC designs. This article seeks to develop a POPBL conceptual framework for the design and implementation of ASICs. To this effect, a content analysis of scientific literature, models and frameworks were carried out with a focus on ASIC application, design and implementation, PbBL, PjBL, and POPBL processes. The resulting conceptual framework is a logical and systematic algorithm starting from problem identification/analysis, activation of prior knowledge, the setting of objectives/specifications, project initiation/execution, assessments/evaluation, and public presentation. The POPBL process stages act as the anchor for the ASIC design and implementation from start, product specifications, architecture, logic design, physical design, and tap-out. The framework will be useful for students and researchers for the development of soft skills like problem-solving, critical thinking, creativity and innovation.

Keywords— Problem-Oriented Learning, Project Based-Learning, Application-Specific Integrated Circuits, Conceptual Framework, Development & Implementation.

I. INTRODUCTION

The increasing demand for complex technology with higher functionality, micro-size devices with lower power dissipation has placed heavy challenges on emerging multimedia and portable electronics industry. This has made the problem of integrated circuit manufacturers so demanding in terms of time-market-circle where shorter design and implementation is carried out within a limited lifetime of products. The advent of Application Specific Integrated Circuits (ASICs) in from of system-on-chip has presented a promising future for addressing these challenges [1]. ASIC has presented promising flexible characteristics with value-added features like super functional performance with high operating speed thus, linking the innovation to the evolution of process technology.

The future of Information Technology (IT) for instance stand to benefits highly from ASIC innovations like machine learning like Google's Tensor Processing Units (TPU) with designs to run key deep learning algorithms as part of the Tensor Flow machine learning framework. In cryptocurrency, the introduction of blockchain ASIC has made the use of Central Processing Units (CPUs) and Graphic Processing Units (GPUs) obsolete as producers like Bitmain are now turning their ASIC expertise into Artificial Intelligence (AI) with a poise to enter Machine Learning as a Service (MLaaS) [2]. The Internet of Things (IoT) now utilizes custom-built ASICs to minimize physical space with low energy function demand, this is in addition to IoT kits that connect with cloud platforms that also run their ASICs. Another promising future of ASIC is Multi-cloud application where today's digital business relies on a hybrid of private cloud, public cloud and on-premises hardware, the premise upon which ASICs can sit either in the cloud or on-premises environment [3]. These and many promising features of ASICs call for the development of a systematic Problem-Oriented Project-based learning theoretical framework to be used as a guide for the development and implementation of ASICs.

II.ASIC DESIGN AND IMPLEMENTATION PROCESS

Like any other system, ASIC design and implementation has various stages of execution to come up with the desired design and specifications and as such, the design flow process is the backbone of every ASIC design process. The entire journey starts from a concept or problem to functional silicon which though in micro-size can perform wonderful functions [4]. The process is as shown in Figure 1.

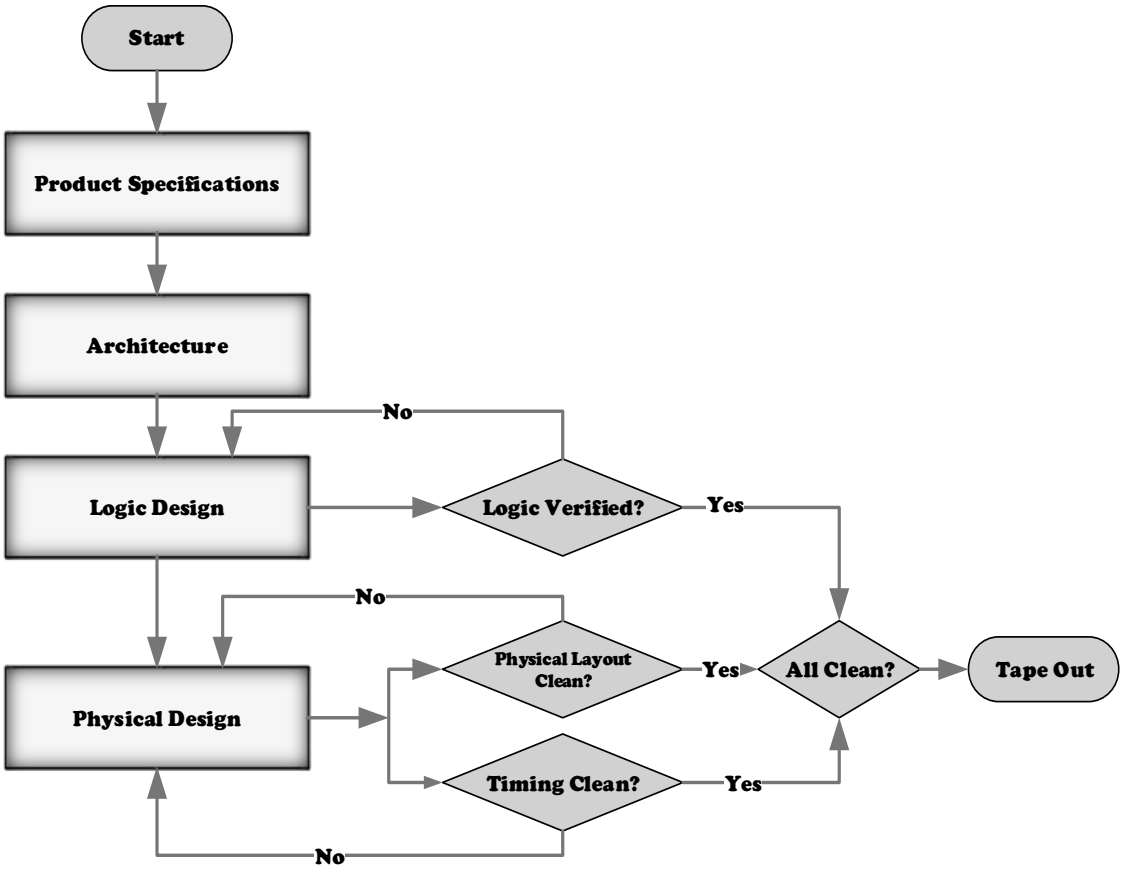

Figure 1: ASIC Design and Implementation Flow

A. ASIC Specifications

The first stage of ASIC design is to define or specify the expected function of the product before embarking on the design. The stage involves a market survey to determine the potential customers and their needs as well as consulting experts to determine the changing and future trends in the industry. The need for consulting experts is to avoid duplications and possibly, legal cases resulting from piracy or plagiarism, knowing that most ASIC designs and patterns last between 6 to 24 months. The market survey aims to enable ASIC designers to come up with top quality product specification with high market and demand value. The survey also ensures attainment of specific computing algorithm to be implementations, clock frequencies to make the product more receptive to end-users, Package type-Ball Grid Array (BGA) or Chip Scale Package (CSP) and so on [5]. It also helps in determining the power supply, intended temperature range be produced and the communication protocols to be used as an interface with the environment. The need for a thorough and accurate specification is necessary to as it sets a firm foundation for the ASIC design

B. ASIC Architecture

The ASIC specification is followed by the partitioning of the ASIC into various functional blocks as designers brainstorm on various possible options for the design with detailed discussion on the pros and cons as well as consideration for the performance implications, allocation of resources in terms of time and cost, and technical feasibility [6]. The quality of the design depends on the ASIC chip's best performance with minimal hardware resources as well as limiting the cost within the proposed budget. This stage entails a detailed breakdown of functional blocks with time and budget allocation. A detailed defined functional block helps in identifying critical modules and brainstorming whether there is a need for the re-use of previous project intellectual properties (IPs), modify the previous IPs or procure new ones [1].

C. Logic Design and Verification

The logic design and verification stage involve data flow and coding of every functional block hardware description language such as Verilog, System Verilog or VHDL, this interactions between functional blocks must be coded [5], [7]. The logical design usually involves:

i. ***Combinational Logic*** where Boolean combinational gates like the AND, OR, NAND, NOR, XOR and so on are combined to perform complex digital tasks.

ii. ***Sequential Elements*** that act as an interface between various combinational logic clouds that perform various functions through temporary storage of output. Bi-stable sequential elements like flip-flops are utilized as memory elements which are controlled by a controlled or synchronizing signal usually referred to as clock.

iii. ***Finite State Machines (FSMs)*** which is an advanced format for the design of highly complex digital circuits where circuit functions are broken down into various states and logics that determine the timing of system's movement from one state to the other. This is usually carried out through designs of state diagrams which consists of nodes that represent the states and edges that enable the transition from one state to the other.

iv. ***Arithmetic Logic Blocks (ALBs)*** also known as Arithmetic Logic Unit (ALU), ALBs are digital circuits that perform logical arithmetic operations and are basic building blocks for the central processing unit (CPU) in computer systems. The arithmetical operations are accomplished through transistor switches to manipulate binary digits 0 and 1where one transistors control the second one.

Logic designers can utilize the most suitable application for the optimization of various parameters.

v. ***Data-Path Design*** takes care of interconnections between logic cells with a regular layout that produces predictable and equal delay as well as creates an interconnection between cells that build into each cell. Elements of data-path include adders, shifter, and multipliers and so on.

vi. ***Analog Design*** ASICs also utilize many analogue systems in addition to digital logic to enable interface with the environment by utilizing various sensors, Analog to Digital Converters (ADCs) and Digital to Analog Converter (DACs).

D. Physical Design

The physical design stage is the backbone of any ASIC design process and is broken down into individual steps. To have a successful design, a good understanding of the ASIC specification and requirement, a silicon-proven ASIC flow, and good understanding and Utilization of Electronic Design Automation (EDA) tools are required [8]. The process as shown in Figure 2 involves several stages and each stage must be correctly carried out since subsequent corrections could be costly. Every process must be completed satisfactorily with the required stage incorporated before proceeding to the next. It is also necessary to ensure the full functionality of the ASIC design process interface [1].

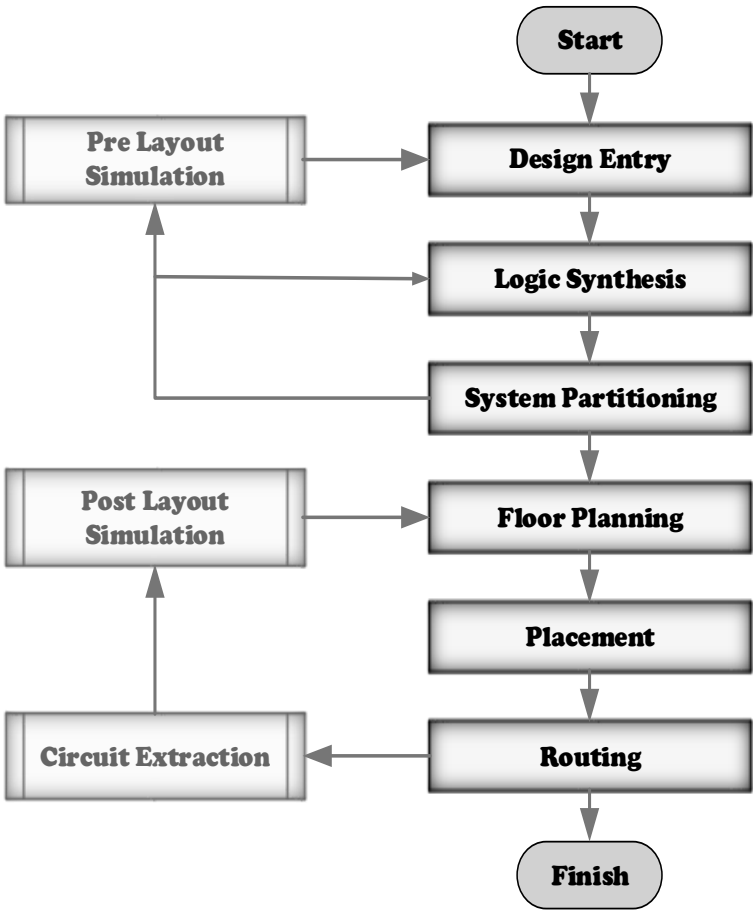

Figure 2: ASIC Physical Design Flow

The ASIC physical layout involves various factors ranging from the most commodious proximity of particular parts of the circuit passage times to various networks that are required to be made across various sections. Normally, the layout is usually carried out under the control of a computer however; restrictions are placed on the physical to ensure the attainment of certain electrical parametric quantities.

i. ***ASIC simulation and modelling:*** The most important factor is to correctly meet the design specifications after the design has been captured and this is ascertained through further simulation. The previously generated software is used to check ASIC design because the discovery of many errors in the output integrated circuit is errors that are functional at the modelling stages. Also, a critical check of the timing is necessary, particularly in customized ASIC designs. This has to be carried out on temperature range, estimated process variations, and input voltages that are slightly higher than the specified values. [9].

ii. ***Formal verification:*** There is the increasing importance of this stage of ASIC design in recent years. To ensure the correctness of the design, a formal verification must be carried out considering the growing ASIC design complexities [4]. Meta stability between various ASIC design clock areas as well as clock skew are the aspects that must be checked to ensure the correct functioning of all the variables within a software model. [9].

iii. ***ASIC test techniques:*** The next stage after manufacture is the testing of the ASIC device which is usually carried out using three techniques. The first is boundary scan, JTAG, IEEE1149.1 which involves the checking of the device internal circuitry and the input/output areas [1]. This technique is slow and not suitable for complex devices due to its serial nature. The second technique utilizes termed scan chains where ASIC existing register is used with each incorporating a multiplexer between the scan and normal input. With this approach, series of chains are set up with each having two inputs and one output and the process involves the generation of test vectors for inputs thus, making it possible carry out output error analysis. The third technique is the Built-in Self-Test (BIST). This is applicable in the test of chips incorporating elements such as SRAM which take a long time to check. Due to their cost-effectiveness in terms of silicon area and test time, the technique and extent of these vectors can often influence the choice of a vendor [9].

iv. ***Physical test of prototype ASICs*** When the ASIC physical prototype is ready, it is necessary to carry out a complex test which includes testing of ASIC within the target circuit. This includes operational check as well as the process spread to ascertain the production's likely yield. Several techniques are used in problem investigation such as boundary scan where complex tools are used and checks are carried out around the interface to the external circuitry [9]. Some other techniques involve symptoms investigation and hypothesis generation which are tested against ASIC simulation. This allows for the simulation of correct problems simulation and correction.

v. ***Lifecycle reviews & handover to manufacturing:*** As with any user interface within sections or various units of a development team, it is mandatory to ascertain that the interfaces function optimally and that all the required information is passed correctly passed over. This is peculiarly true of the interface with the silicon vendor as they form a different company and will have various processes of

operation. To achieve this, the handover of information to and from the ASIC design service is normally done on a formal basis, and the silicon vendors will often expect to see many items including the verification results for the ASIC design, as part of this [9].

III. PROBLEM-ORIENTED PROJECT-BASED LEARNING (POPBL)

Problem-Oriented project-based Learning (POPBL) aims at providing solutions to the problems of the society as well as enhances learners' creativity through the initiation and execution of a project. The experience from the process promotes learners' acquisition of knowledge from the research, findings, and discoveries [10]. This method is learners' centred, therefore, it doesn't require the memorization of formulas or theories but enhances the acquisition of creative and analytical thinking through the analysis information acquired to solve the existing problem [11], [12]. As a problem cantered process, POPBL focuses on tailoring the content of the curriculum around the problem setting instead of subject or courses [13]. The process engages learners with complex settings with the skills and information needed to manage a given situation [14], [15].

According to [14], POPBL is characterized by active learning participation and cooperative groups' project work, guided participation in negotiation between learners and the instructor as a facilitator and supervisor. It enhances the cross-disciplinary acquisition of knowledge across academic fields. The take-off point for a POPBL is the inquiry stage where students or learners groups investigate a problem is not known to them thereby, provoking their thoughts for action [10], [16], [17]. In the process of attempting a solution to a given problem, groups embark on organized and logical dialogue approach through the collection relevant materials and information; utilize applicable theories and methods as guides to systematically transform and orchestrate the materials or information to discover and elucidate the problem domain as well as research questions. This is followed by coming up with conclusions that constitute variations in knowledge within the learners, thereby resulting in a product through which their diverging insights are intercommunicated to others.

The respective members of the team together in negotiation with the facilitator engage on how to develop a functional research question, the choice of theory as well as constructs and decide on the approach to be utilized and the subject for the analysis. To enable students or learners to consolidate their wider study competence, the initiated project work must be exemplary by utilizing methods, analytical and methodological comprehension as well as work with concepts and theories that go outside the given project. The aim is to help students to integrate their findings and the knowledge acquired in their previous experiences and utilize them in developing new experiences and skills as well as providing solutions to new problems.

A. POPBL Process

POPBL procedures could be attained through the individual procedures of PbBL and PjBL. These include problem identification/analysis, applicable and alternative solutions, implementation and construction of the proposed components, and final testing of the project for quality assurance [10], [12], [16]. [12], divided the process into three main stages: Problem analysis and design, Development & Testing, and Re-development (Evolution) & Testing.

i. ***Problem Orientation & Analysis:*** This stage of POPBL aims at reaching an ample serious comprehension of the given problem to ascertain that students are sure that their solution is adequate for addressing the problem. Understanding a given problem demands that you already know a setting that could be completely new for you - and acknowledging the imbalances in the setting. So to understand a situation, you have to study other agents and the people that view the situation troubling [10].

ii. ***Activation of Prior Knowledge:*** Once a given problem is examined and the root causes are discovered, the next phase is for the students to review their previous knowledge to determine their level of readiness to tackle the problem. This is carried out as soon as the essential thinking framework was actuated through direct recall, define, or even by manifesting to very important final knowledge or experience. Prior activation of knowledge can serve as a basis for newly acquired expertise on group members [18]–[20], the students' group focus on that knowledge supplied with fresh used knowledge which activates the previously acquired knowledge as well as relates the intellectual competence of the students.

iii. ***Research & Learning Objectives****:* Having activated the prior knowledge, students embark on further research to complement their previous knowledge. The objective of the given problem is now defined to guide the attainment of new skills and knowledge based on the set objectives. The objective clearly defines the quality and quantity of an attainable target's performance within the given time and resources [24]. These objectives are not necessarily intended to be measured but instead, serve as a road map of the target result.

iv. ***Project Initiation and Execution:*** After conducting complementary research and the objectives spelt out, a project is initiated to achieve the set objectives. Project initiation and execution have no distinct process nor stages since various projects originate from different problems and have distinct objectives that define the steps to be taken [25]. POPBL process of learning begins with the output result as the set goal and the team members follow a chosen procedure to arrive at the result or product.

v. ***Assessment/Evaluation:*** to ensure that the aims and objectives of a course are achieved, formative assessment and evaluation are carried out throughout the process. Since this aims at giving students concept understanding, they are expected to sustain it through experience instead of standardized tests. The nature of assessment here is open-ended and could be written and/or oral in group or individual. Another paramount measure utilized is a weekly reflective journal which applies a metacognitive approach. In this measure, students are sharing their learning process. In other words, they are carrying out self-evaluation on their learning process. Students' efforts, analytical skills, creativity/innovation, leadership, and teamwork are measured using portfolio assessment [16].

vi. ***Public Presentation:*** The presentation of the project to the public is a last and crucial stage of POPBL as the method aims at addressing the societal problems through the initiation and execution of the project. Presentation skills are very vital both within and outside the classroom [26], [27]. After the project has been completed, a public presentation is a platform for the team members to share with the audience what has been achieved. It also opportune students to challenge and expand on their knowledge of the topic by welcoming and responding to questions from others [28]. A confident presenter in the world of work can communicate, inform and motivate colleagues effectively. To get the students listening to each

other, the audience can be set as a task with a set of questions being answered in a presentation [29].

IV. POPBL-ASIC DESIGN AND IMPLEMENTATION FRAMEWORK

The POPBL-ASIC design and implementation framework is a logical algorithm that is aimed at systematically guiding creativity and innovations in the development of ASICs. As shown in Figure 3, the process which starts with problem identification and analysis helps in the identification of a problem that is to be addressed by an intended ASIC. This helps students and ASIC developers to identify a problem from the society or an existing ASIC to identify the root causes(s) of the problem as well as explore possible solutions in a logical way and team approach. This is followed by the activation of prior knowledge where students or developers review their aptitude as well as to conduct further research to enable them to gather the needed knowledge and skills necessary for addressing the problem. All these mark the start stage of ASIC design and implementation. Having gathered the necessary resources, the next stage is a set of objectives based on the given problem, the remote causes and the expected output. This is carried out at the product specification stage of ASIC design and implementation process. With objectives and ASIC specification in place, the next stage is the project initiation and implementation which involves architecture, logic design and physical design of ASIC.

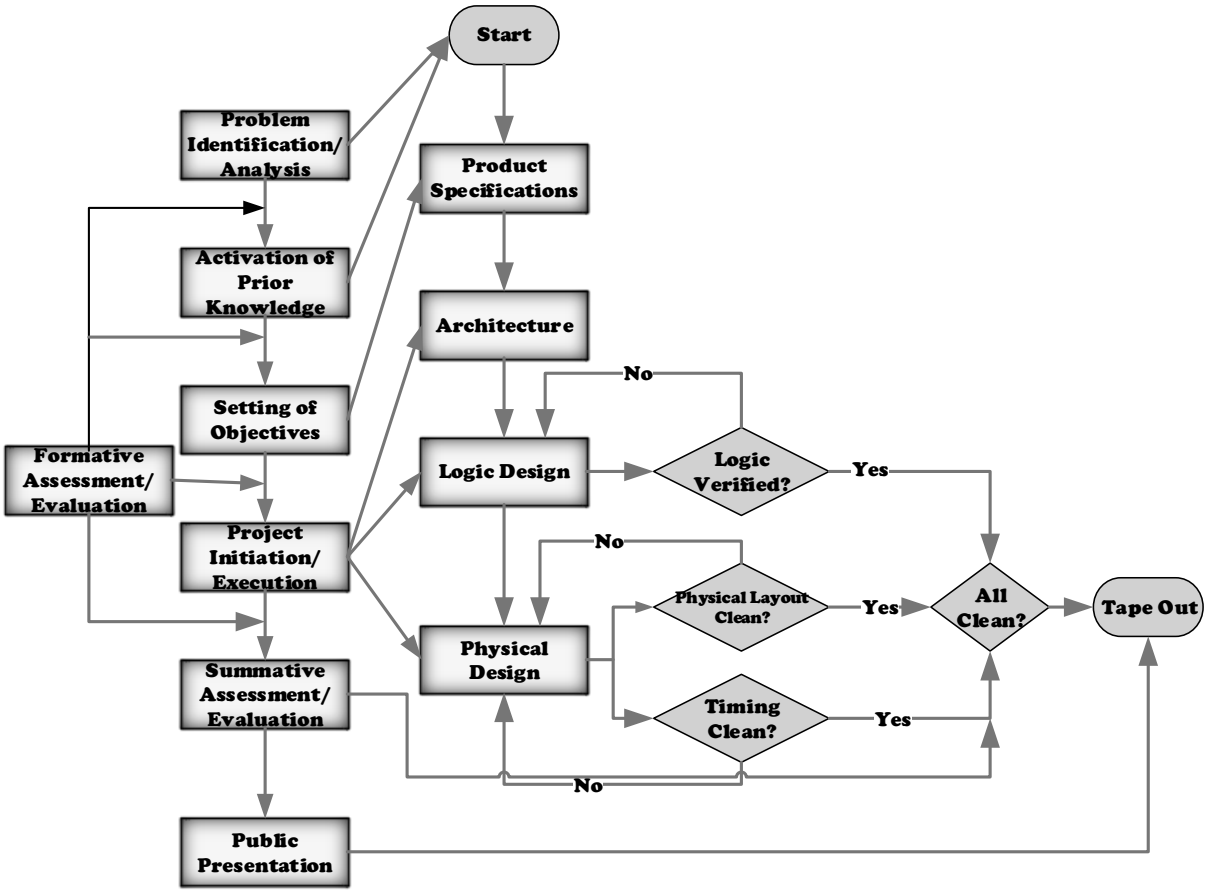

Figure 3: POPBL-ASICs Design and Development Framework

The process involves continues evaluation at every stage to ensure that the objectives and specifications at every stage are met through a formative assessment and evaluation. At the end of the process, a summative assessment and evaluation are carried out to determine the functionality of the developed ASIC based on the set objectives. The parameters to must be considered include logic verification, physical layout cleanliness, and timing cleanliness. This followed by a public presentation to the audience who are the likely beneficiaries of the developed ASIC. This process helps students and developers to be collaborative, logical, critical, creative and innovative.

V. CONCLUSION

The development of a POPBL-ASICs design and implementation framework is based on the application popularity of ASICs in the 21sts century. The analysis revealed the relevance and impact of ASICs on IT innovations like Machine Learning, Tensor Processing Units, Machine Learning as a Service, Internet of Things, Central Processing Units, and Graphic Processing Units. The analysis also revealed the logical flows for the development of ASICs which were interfaced with the process of POPBL to arrive at a framework which can serve as an algorithm for innovations the design and implementation of ASICs. Based on the analysed literature, the resulting framework has the potentials of developing 21st-century skills like problem-solving. Teamwork, creativity, critical thinking, and innovation skills

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