Available Online at www.ijcsmc.com

International Journal of Computer Science and Mobile Computing

A Monthly Journal of Computer Science and Information Technology

ISSN 2320–088X

IJCSMC, Vol. 2, Issue. 9, September 2013, pg.268 – 278

RESEARCH ARTICLE

Power Efficient Design of Sequential Circuits using OBSC and RTPG Integration

Rampriya.R[1], Marutharaj.T[2]

[1]PG Scholar/ M.E VLSI Design, TKSCT, Theni, India

[2]Assistant Professor, Department of ECE, TKCST, Theni, India

[1] rampriya.28.1991@gmail.com; [2] maruthuraj@gmail.com

Abstract—In Integrated circuits a gargantuan portion of chip power is expended by clocking systems which comprises of timing elements such as flipflops, latches and clock distribution network. This paper enumerates power efficient design of shift registers using TSPC flipflops along with Clock and Power gating integration. Clock gating and power gating proves to be very effective solutions for reducing dynamic and active leakage power respectively. The two techniques are coupled in such a way that the clock gating information is used to drive the control signal of power-gating circuitry. In this paper, an activity driven fine-grained clock and power gating is proposed. First, a technique named Optimized Bus-Specific-Clock-Gating (OBSC) is introduced which reduces the problem of gated flipflop selection by appropriate selection of subset of flipflops. Then another technique named Run Time Power Gating (RTPG) is proposed for power gating the combinational logics performing redundant operations. The proposed shift registers are designed up to the layout level with 1V Power supply in 90nm technology and simulated using microwind simulations for different clock frequencies and the performance of the shift registers are evaluated by observing the average power, delay and PDP.

Keywords— Flip Flop; CMOS; TSPC; OBSC; RTPG; PDP

Full Text: http://www.ijcsmc.com/docs/papers/September2013/V2I9201367.pdf